THE UNIVERSITY OF TEXAS AT DALLAS
Erik Jonsson School of Engineering and Computer Science
Department of Electrical Engineering

EE/CE 6302: Microprocessor Systems

(Fall 2007, Tuesday and Thursday: 1:00–2:15 p.m., ECSS 2.415)

1 General Information

Instructor:	Mehrdad Nourani
Office & Phone:	ECSN 4.924, 972-883-4391
E-mail (Webpage):	nourani@utdallas.edu (http://www.utdallas.edu/~nourani)
Office Hours:	Tuesday and Thursday 3:00–4:00 p.m., or by appointment.
Required Text:	*None.*
References:	1. Related papers, articles, datasheets from literature and internet.
	2. *The 8051 Microcontroller and Embedded Systems*, M. Mazidi and J. Mazidi, Prentice Hall, 2000.
	3. *Network Systems Design Using Network Processors*, Douglas Comer, Prentice Hall, 2003.
	4. *Modern Microprocessors*, V. Korneev and A. Kiselev, Charles River Media, 2004.
Course Web Page:	http://webct.utdallas.edu/
Teaching Assistant:	To be announced.

2 Catalog Description

EE 6302: Microprocessor Systems (3 semester hours).
Design of microprocessor based systems including I/O and interface devices. Microprocessor architectures. Use of emulators and other sophisticated test equipment. Extensive laboratory work.
Prerequisite: EE 4304 or equivalent and background in VHDL/Verilog. (2-3) Y

Note: All students are required to also register for one of the two microprocessor lab sessions, i.e. EE/CE6302.002 and EE/CE6302.001 on Thurs. 2:30-5:30 pm and 5:30-8:30 pm, respectively. These labs are needed throughout the semester for training on the microprocessor boards and also doing your projects.

3 Course Objective

The objective of this graduate level course is to introduce the architecture and design methodologies of processors and processor-based embedded systems. We provide students with access to the embedded system laboratory where they can use 8051 microcontroller boards (from Systronix, Inc.) and NIOS Stratix reconfigurable processor (from Altera Corporation) to create and design various processor-based systems. Through projects, it is expected that the students will acquire a clear understanding of both the behavioral (e.g. software) and structural (e.g. hardware) techniques and strategies for developing embedded systems including packet-based network devices. In particular, students are expected to be able to:

- identify the basic architecture and internal structure of a microprocessor or microcontroller
- develop system specifications that require embedded microprocessors
- learn how modern microprocessor design is performed using various CAD tools
- distinguish datapath and controller in a processor system and its RISC/CISC platform
- write assembly language programs and work with I/O interfaces, timers, interrupts and serial ports
- work with Intel 8051 microcontroller board to develop small projects
- work with Altera NIOS II processor as a reconfigurable processor to develop small projects
- develop individual subsystem engines using VHDL/Verilog and integrate it with Altera NIOS
- learn algorithms for packet processing systems and integration techniques
- perform hardware and/or software test and evaluation for processor-based system
- document the activities and prepare informative technical reports

4 Grading

Grading will be based homeworks and projects as follows:

Homeworks/Labs:	15% (Throughout the semester)
Midterm Test:	20% (Thur. 11-1-2007)
Project 1:	15% (Thur. 9-13-2007)
Project 2:	15% (Thur. 10-4-2007)
Project 3:	15% (Thur. 10-25-2007)
Project 4:	20% (Thur. 11-15-2007)

5 Course Policy

- **Homeworks & Projects:** Homeworks and projects will be assigned throughout the semester, and will be due approximately once every two weeks at 1:00 p.m. at the *beginning* of the lecture/lab period. Some of the homeworks/projects require programming, using 8051/NIOS microcontroller/microprocessor boards or using CAD tools for design, implementation, simulation and analysis. To have enough time start as early as possible. You can work on the projects individually or in a group of two.
- **Late/Missed Submission:** A homework/project is considered *late* if it is turned in after 1:00 p.m. of the due date. There will be 30% per day penalty for late homeworks up to 2 days excluding weekends and holidays. Late homeworks and reports won't be accepted after 2 days. Make-up option for late or missed tests, reports, demos or presentations will not be accepted unless the student has obtained permission from the instructor *before* the due date. Permission will not be given without documentation of truly exceptional circumstances.
- **Laboratory:** The *Embedded System Laboratory* (ECSN 3.118 and ECSN 3.120) will be available to the students to help them with their hardware implementation. Some key lab equipments such as PC hosts with some general-purpose softwares, oscilloscope, logic analyzer, function generator, power supply, PROM programmer and eraser, etc. will be available during the lab hours (to be announced in the web page). The 8051 boards (from Systronix, Inc.) and NIOS Stratix reconfigurable processor (from Altera Corporation) are also available in the lab.
- **Report/Demo/Presentation:** You need to prepare a technical report for each project. These documents should show clearly your work and investigation/design process. For some of the projects short demo or presentation may be required. on the due dates.
- **Attendance:** Announcements and complementary materials will be posted on the course web page. However, regular attendance and taking notes are highly recommended.

6 Syllabus & Tentative Lecture Plan

Weeks		*Readings*	*Topics Coverage*
Tues.	*Thur.*		
	8/16		Introduction: course introduction; technologies and style; y-chart; role of CAD; present and future of networking and packet processing;
8/21	8/23	Architecture Book	Microprocessor Systems: Data path and controller path microarchitectures; RISC and CISC; parallelism techniques; application specific processors;
8/28	8/30	8051 Datasheet & Ref. 2	Case study of the 8051 microcontroller: architecture; assembly language; I/O port access; jumps and loops; procedure calls; timer/counter programming
9/4	9/6	8051 Board Manual, Ref. 2	interrupts; strobing versus handshaking; serial communication; Training Lab Session
9/11	9/13	Ref. 1 & Ref. 3	Computer Networking Essentials: packet switching technology and networks; Network Processors: applications; market demand; network tasks;
9/18	9/20	Ref. 1 & Ref. 3	physical components of network; using processors in modem, network interface card, hubs and router;
9/25	9/27	Ref. 1 & Ref. 3	IP routing: principles; algorithms; architectures; Invited Speaker
10/2	10/4	NIOS Board Manual	ASIC versus ASIP; reconfigurable architectures; system-level design; Training Lab Session
10/9	10/11	NIOS Board Manual	Hardware modeling and design using HDL Invited Speaker
10/16	10/18	NIOS Board Manual	Reconfigurable processors: methodologies; structures; System level design & test issues: partitioning; estimation;
10/23	10/25	Ref. 1	Challenges in instruction set design; co-processor versus processor redesign; Challenges in packet processing: table lookup; forwarding engine;
10/30	11/1	Ref. 1 & Ref. 3	CAM-based architectures; switch fabric structures; packet classification and scheduling; Midterm Test
11/6	11/8	Ref. 1	System-on-Chip: concept; issues on design, test, power, etc.; SoCs with embedded processors;
11/13	11/15	Ref. 4	Case studies and miscellaneous topics Demo and Presentation
11/20	11/22	Ref. 4	processor case studies. Thanksgiving (university holiday).

7 Field Trip Policies

Off-campus Instruction and Course Activities

Off-campus, out-of-state, and foreign instruction and activities are subject to state law and University policies and procedures regarding travel and risk-related activities. Information regarding these rules and regulations may be found at the website address http://www.utdallas.edu/BusinessAffairs/Travel_Risk_Activities.htm. Additional information is available from the office of the school dean. Below is a description of any travel and/or risk-related activity associated with this course.

8 Student Conduct & Discipline

The University of Texas System and The University of Texas at Dallas have rules and regulations for the orderly and efficient conduct of their business. It is the responsibility of each student and each student organization to be knowledgeable about the rules and regulations which govern student conduct and activities. General information on student conduct and discipline is contained in the UTD publication, A to Z Guide, which is provided to all registered students each academic year.

The University of Texas at Dallas administers student discipline within the procedures of recognized and established due process. Procedures are defined and described in the Rules and Regulations, Board of Regents, The University of Texas System, Part 1, Chapter VI, Section 3, and in Title V, Rules on Student Services and Activities of the university's Handbook of Operating Procedures. Copies of these rules and regulations are available to students in the Office of the Dean of Students, where staff members are available to assist students in interpreting the rules and regulations (SU 1.602, 972/883-6391).

A student at the university neither loses the rights nor escapes the responsibilities of citizenship. He or she is expected to obey federal, state, and local laws as well as the Regents' Rules, university regulations, and administrative rules. Students are subject to discipline for violating the standards of conduct whether such conduct takes place on or off campus, or whether civil or criminal penalties are also imposed for such conduct.

9 Academic Integrity

The faculty expects from its students a high level of responsibility and academic honesty. Because the value of an academic degree depends upon the absolute integrity of the work done by the student for that degree, it is imperative that a student demonstrate a high standard of individual honor in his or her scholastic work.

Scholastic dishonesty includes, but is not limited to, statements, acts or omissions related to applications for enrollment or the award of a degree, and/or the submission as one's own work or material that is not one's own. As a general rule, scholastic dishonesty involves one of the following acts: cheating, plagiarism, collusion and/or falsifying academic records. Students suspected of academic dishonesty are subject to disciplinary proceedings.

Plagiarism, especially from the web, from portions of papers for other classes, and from any other source is unacceptable and will be dealt with under the university's policy on plagiarism (see general catalog for details). This course will use the resources of turnitin.com, which searches the web for possible plagiarism and is over 90

10 Email Use

The University of Texas at Dallas recognizes the value and efficiency of communication between faculty/staff and students through electronic mail. At the same time, email raises some issues concerning security and the identity of each individual in an email exchange. The university encourages all official student email correspondence be sent only to a student's U.T. Dallas email address and that faculty and staff consider email from students official only if it originates from a UTD student account. This allows the university to maintain a high degree of confidence in the identity of all individual corresponding and the security of the transmitted information. UTD furnishes each student with a free email account that is to be used in all communication with university personnel. The Department of Information Resources at U.T. Dallas provides a method for students to have their U.T. Dallas mail forwarded to other accounts.

11 Withdrawal from Class

The administration of this institution has set deadlines for withdrawal of any college-level courses. These dates and times are published in that semester's course catalog. Administration procedures must be followed. It is the student's responsibility to handle withdrawal requirements from any class. In other words, I cannot drop or withdraw any student. You must do the

proper paperwork to ensure that you will not receive a final grade of ”F” in a course if you choose not to attend the class once you are enrolled.

12 Student Grievance Procedures

Procedures for student grievances are found in Title V, Rules on Student Services and Activities, of the university’s Handbook of Operating Procedures.

In attempting to resolve any student grievance regarding grades, evaluations, or other fulfillments of academic responsibility, it is the obligation of the student first to make a serious effort to resolve the matter with the instructor, supervisor, administrator, or committee with whom the grievance originates (hereafter called ”the respondent”). Individual faculty members retain primary responsibility for assigning grades and evaluations. If the matter cannot be resolved at that level, the grievance must be submitted in writing to the respondent with a copy of the respondent’s School Dean. If the matter is not resolved by the written response provided by the respondent, the student may submit a written appeal to the School Dean. If the grievance is not resolved by the School Dean’s decision, the student may make a written appeal to the Dean of Graduate or Undergraduate Education, and the deal will appoint and convene an Academic Appeals Panel. The decision of the Academic Appeals Panel is final. The results of the academic appeals process will be distributed to all involved parties.

Copies of these rules and regulations are available to students in the Office of the Dean of Students, where staff members are available to assist students in interpreting the rules and regulations.

13 Incomplete Grade Policy

As per university policy, incomplete grades will be granted only for work unavoidably missed at the semester’s end and only if 70% of the course work has been completed. An incomplete grade must be resolved within eight (8) weeks from the first day of the subsequent long semester. If the required work to complete the course and to remove the incomplete grade is not submitted by the specified deadline, the incomplete grade is changed automatically to a grade of F.

14 Disability Services

The goal of Disability Services is to provide students with disabilities educational opportunities equal to those of their non-disabled peers. Disability Services is located in room 1.610 in the Student Union. Office hours are Monday and Thursday, 8:30 a.m. to 6:30 p.m.; Tuesday and Wednesday, 8:30 a.m. to 7:30 p.m.; and Friday, 8:30 a.m. to 5:30 p.m. The contact information for the Office of Disability Services is:

The University of Texas at Dallas, SU 22
PO Box 830688
Richardson, Texas 75083-0688
(972) 883-2098 (voice or TTY)

Essentially, the law requires that colleges and universities make those reasonable adjustments necessary to eliminate discrimination on the basis of disability. For example, it may be necessary to remove classroom prohibitions against tape recorders or animals (in the case of dog guides) for students who are blind. Occasionally an assignment requirement may be substituted (for example, a research paper versus an oral presentation for a student who is hearing impaired). Classes enrolled students with mobility impairments may have to be rescheduled in accessible facilities. The college or university may need to provide special services such as registration, note-taking, or mobility assistance.

It is the student’s responsibility to notify his or her professors of the need for such an accommodation. Disability Services provides students with letters to present to faculty members to verify that the student has a disability and needs accommodations. Individuals requiring special accommodation should contact the professor after class or during office hours.

15 Religious Holy Days

The University of Texas at Dallas will excuse a student from class or other required activities for the travel to and observance of a religious holy day for a religion whose places of worship are exempt from property tax under Section 11.20, Tax Code, Texas Code Annotated. The student is encouraged to notify the instructor or activity sponsor as soon as possible regarding the absence, preferably in advance of the assignment. The student, so excused, will be allowed to take the exam or complete

the assignment within a reasonable time after the absence: a period equal to the length of the absence, up to a maximum of one week. A student who notifies the instructor and completes any missed exam or assignment may not be penalized for the absence. A student who fails to complete the exam or assignment within the prescribed period may receive a failing grade for that exam or assignment. If a student or an instructor disagrees about the nature of the absence [i.e., for the purpose of observing a religious holy day] or if there is similar disagreement about whether the student has been given a reasonable time to complete any missed assignments or examinations, either the student or the instructor may request a ruling from the chief executive officer of the institution, or his or her designee. The chief executive officer or designee must take into account the legislative intent of TEC 51.911(b), and the student and instructor will abide by the decision of the chief executive officer or designee.

These descriptions and timelines are subject to change at the discretion of the Professor.