EE/CE 3320 DIGITAL CIRCUITS, Spring 2020
Electrical and Computer Engineering
Erik Jonsson School of Engineering & Computer Science at UTD

Professor: Tooraj Nikoubin
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Office Hours: MW 11:30am – 12:30pm
Tu 9:00am – 10:00pm or by appointment
Room: ECSN 3.904, (972)883-4759

Location: ECSS 2.415
Time: MW 10:00am–11:15am

TA: see elearning
TA Email: see elearning

Course Description

The importance of digital circuits and systems cannot be overestimated in present day and age. Digital circuits form the basis for most of the electronic devices ranging from small electronic toys to large scale computers. Hence it is useful to understand how these circuits are designed and operate. All digital circuits operate using the same concepts that will be presented in this class. The only difference is in the complexity of the circuits.

Course Pre-requisites

Prerequisites: EE 2310

Course Learning Objectives

- Ability to design, analyze, and optimize combinational logic circuits
- Ability to design, analyze, and optimize synchronous sequential logic circuits
- Ability to conduct timing analysis on combinational and sequential logic circuits
- Ability to understand and apply practical aspects of digital design including datapath components
- Ability to understand logic gate implementations and their electrical properties

Course Material

- **Required Text Book:**

- Charles H.Roth, Jr. and Larry L. Kinney, "Fundamentals of Logic Design"

- **References:**

- Frank Vahid: *Digital Design –with RTL Design, VHDL, and Verilog,* John Wiley Publishers. Second Edition, ISBN: 978-0-470-53108-2.
- S. Brown and Z. Vranesic, *Fundamentals of Digital Logic With Verilog Design*, McGraw-Hill Publishing. Second Edition, 2008

- All announcements and homework assignments will be posted online for this course. It is the responsibility of each student to check this web page at least once a week for new announcements and homework.

Academic Calendar

- First Class Day: Monday, Jan. 13, 2020
- Last Class Day: Wednesday, April. 30. 2020
- Spring Break: March. 16 to 22, 2020
- 1st Exam: Monday Feb 17th 10:00am – 11:15am, ECSS 2.415,
- 2nd Exam: Monday Mar 23th 10:00am – 11:15am, ECSS 2.415,
- 3rd Exam: Final Exam schedule TBA (May 2 or 8)

• Course Announcements and Homework Assignments

Course announcements and homework assignments will be posted on the web page for this course and will not be handed out in the class. Sometimes homework provides practice to solve difficult problems. Students are welcome to discuss homework with the instructor and teaching assistants.

• Grading Policy

Final grades in this course will be based on several homework assignments and two examinations given throughout the semester and a final examination. No makeup examinations will be offered in this course. Any graded work can be disputed in writing *within one week* of the return of that work. Complete work will be re-graded.
The grading policy is:

	Course Requirements and Corresponding Weight	
1	Test # 1	15%
2	Test # 2	15%
3	Final exam	35%
4	Project	10%
5	Homework and Quiz	25%

• UT Dallas Policies and Procedures

For all issues related to sharing confidential information, student conduct and discipline, academic integrity, student grievance, incomplete grade, and other student related university policies please refer to this page: http://go.utdallas.edu/syllabus-policies

• List of Topics (subject to base on the progress of the class)

No.	Topic	Text Section # [Online Section #]
1	**Introduction**	**PPT**
2	**Digital Logic Design Fundamentals (Review)** a. *Review*: Truth tables, Boolean algebra and algebraic proofs, AND-OR, OR-AND, NAND, NOR, XOR, XNOR circuits d. Logic minimization (SOP and POS forms) e. Karnaugh Map f. Transistor Level Realization of the logic gates g. Timing analysis of the circuits	 PP. 1-12, 36-52, pp. 94-104 pp. 134-153 **PPT** **PPT**
3	**Quine-McClusky Method**	pp. 173-184
4	**Multi-level gate circuits** a. AND-OR, OR-AND (AOI & OAI) b. NAND-NAND & NOR-NOR configurations c. Other configurations	pp. 199-217 **PPT** 206 **PPT**
5	**Combinational circuit design and simulation** a. Design of the circuit with limited fan-in b. Gate delays and timing diagrams **c.** Hazards in combinational logic	pp. 229-242 229 232 240
6	**Multiplexers, Decoders, and Programable Logic Designs** a. Multiplexers b. Three-state buffers c. Decoders and Encoders d. Read-Only Memories e. Programable Logic devices f. Complex programable logic devices g. Field-Programable Gate Arrays c. Binary Adders and Subractors, d. Comparators	pp. 260-285 261 265 268 271 275 280 282 **PPT** **PPT**
7	**Coding** a. BCD, Aiken, Excess 3, Gray, and some other codes	**PPT**

	b. Code converters (like Decimal to BCD convertor) c. 7-segment display d. Even parity and error detection e. BCD Adder and subtractor	
8	**Combinational logic design using Verilog** Hamming with even parity (First Project)	(Video Tutorials) **PPT**
9	**Latches and Flip-Flops, Buffer, shift Register** a. Set-Reset Latch b. Gate Latches c. Edge-Triggered D Flip-Flop d. S-R Flip-Flop e. J-K Flip-Flop f. T Flip-Flop g. Buffer, Shift Register	pp. 331-354 338 342 346 349 350 351 380
10	**Counters and Counter design** a. Design of BCD Counter b. Design of Binary Counter c. Count up and Count down counter d. Counter design with D, T, RS and JK Flip-Flops e. Counters for other sequences	 **PPT** 384 **PPT** 395 389
11	**Analysis of clocked sequential circuits** a. Frequency dividers b. Timing analysis of counters c. Timing analysis of synchronous and asynchronous circuits g. Sequential logic design using Verilog Programable Timer (Second Project)	**PPT** **PPT** **PPT** **PPT** Video Tutorial **PPT**
12	**Derivation of state Graphs and State Tables (State Machines)** a. Design of Sequence Detector d. More complex Design Problems e. Guidelines for Construction of State Graph f. Elimination of Redundant States g. Equivalent states h. Determination of state equivalence using an implication table i. Timing analysis of state machines	453-497 457 463 467 505 507 509 **PPT**
13	**Datapath Components** a. serial adders and subtractors with accumulator b. design of binary multipliers and dividers c. *Review*: Number system b. Signed number representation d. Comparators e. N-bit Multiplexer f. Arithmetic-Logic Unit (ALU) g. Combinational Shifter h. Multipliers and Divider i. Register File j. Counters and Timers k. Fixed-Point Representation & Arithmetic l. Floating-Point Representation & Arithmetic	 629 633 1-8 16 **PPT** **PPT** **PPT** **PPT** **PPT** **PPT** **PPT** **PPT** **PPT**
14	**Advanced Topics** • Hazard, Race, CLK-Skew • Carry Lookahead Adder • Parallelism: Pipelining and Concurrency	 **PPT** **PPT** **PPT**

Note 1: ***Some topics from the course syllabus are not fully covered in any text book.***

Note 2: ***The descriptions and timelines contained in this syllabus are subject to change at the discretion of the Professor.***

Note 3: Syllabus – Corona Modifications for the rest of semester

- **Grading Policy: There is no change on the items and their percentages,**

	Course Requirements and Corresponding Weight	
1	Test # 1	15%
2	Test # 2	15%
3	Final exam	35%
4	Project	10%
5	Homework and Quiz	25%

- **But for the students who may have a problem with Verilog installation on their personal system, you have three following options:**
  1. *Using remote access tools to UTD server for running circuit simulator (Contact your TAs for help)*
  2. *Using another digital circuit simulator for running your project,*
  3. *In worse case, you can replace your project with extra homework for each project*

  In the second and third cases you need to contact your professor before the deadline,

- ***Office hours of Professor, TAs, and Tutors:***
  1. *They will be available during their office hours via Webex or Blackboard Collaborate (in elearning system)*
  2. *You will find a text tutorial on elearning how to use these systems*

- ***Lectures & in-class quizzes: to be continued via Webex (or Blackboard Collaborate) starting April 1***

  In this regard,
  1. *you will have access to your lecture videos two days before class time via elearning/youtube*
  2. *After watching videos: you will provide a list of your questions and upload on the blackboard (this will be recorded as your class activities like quizzes)*
  3. *in-class time: I will answer your questions*
  4. *in-class time: you may have quiz*

- ***Homework, Quiz, second test and final exam date***
  1. *second test date: is April 6th*
  2. *Final exam date: is based on the final exam schedule without change*
  3. *Homework process: via elearning without change*
  4. *In-class quizzes: via elearning*