Course Syllabus

Course Information
CS 4341 Digital Logic and Computer Design

Professor Contact Information
Ivor Page, ECS 4.410, ivor@utdallas.edu

Course Pre-requisites, Co-requisites, and/or Other Restrictions
Prerequisites: EE 2310 or CS 3340, and PHYS 2326. Corequisite: CS 4141.
The following topics are assumed to be known to students:
1. Representation of positive integers by Binary, Octal, and Hexadecimal numbers.
2. Representation of signed integers in 2's complement notation.
3. Addition and subtraction of 2's complement binary integers.
4. Boolean variables and Boolean operations.

Student Learning Objectives

Ability to analyze, minimize, and design gate-level combinational logic circuits using Boolean algebra and 3 and 4-variable Karnaugh maps
Ability to design logic systems using ROM chips, decoders and multiplexers
Ability to design registers and minimized synchronous sequential circuits and counters
Ability to design binary ripple-carry and carry-look-ahead adders
Ability to design time-iterative multipliers and dividers
Understand the MIPS single, multi-cycle, and 5-stage pipelined integer processor
Understand code reordering and loop unrolling to minimize pipeline stalls
Understand branch prediction hardware
Understand multi-level cache memories

Required Textbooks and Materials:
David M. Harris and Sarah L. Harris, *Digital Design and Computer Architecture*. Morgan Kaufmann Publishers, 2nd Ed.

Suggested Course Materials
Notes on eLearning web site for this course.

Assignments & Academic Calendar
(Topics, Reading Assignments, Due Dates, Exam Dates)
See exam dates on the eLearning website.

Tentative Schedule:

Week 1,2 – Boolean Algebra, Karnaugh Maps, Minterm and Maxterm forms, Minimization for 2-level And-Or-Invert, Nand and Nor gate circuits
Week 3 – Cube Algebra and Quine McClusky Minimization Algorithm
Week 4 – Gate Circuits using Decoders and Multiplexers
Week 5 – Flip-flops, Counters, Sequence Generators
Week 6,7 – Synchronous Sequential Circuits (Finite State Machine) design
Week 8 – Registers and Buses, RAM and memory expansion
Week 9 – ALU design, Ripple-carry Adders, Carry Look-ahead Adders
Week 10,11 – Multipliers - Booth Recoding, Radix 2, 4, 8 Recoding; Dividers - Restoring, Non-Restoring.
Week 12 – Instruction-level parallelism, MIPS 5-Stage Pipeline Design, adding multi-cycle functional units, Hazards, Stalls, executing instructions out of order.
Week 13 – Tomasulo's Algorithm, reservation stations.
Week 14 – Reorder buffer and Speculation.
Week 15 – Explicit Register Renaming

Grading Policy
(including percentages for assignments, grade scale, etc.)
Approximate weights for the assignments will be, home works: 15%, Midterm: 35%, final test: 50%. If projects are included (to be decided) these weight will change.

Course & Instructor Policies
(make-up exams, extra credit, late work, special assignments, class attendance, classroom citizenship, etc.)
Makeup exams will only be offered in case of documented illness or other acceptable reason for absence. Prior notification is required where possible.

These course components and timelines are subject to change at the discretion of the instructor.

Please go to http://go.utdallas.edu/syllabus-policies for further university policies.