Course	**CS/TE 4341.003, Digital Logic and Computer Design**
Professor	Richard Goodrum
Term	Spring 2017
Meetings	MW 2:30-3:45 P.M.
Room	ECSS 2.415

Professor's Contact Information

Office Phone	972-883-8830
Other Phone	972-883-2185 (CS Department Phone Number)
Office Location	ECSS 4.604
Email Address	Richard.Goodrum@utdallas.edu
Office Hours	MW 4:00-4:45 or by appointment
Teaching Assistant	Hao Xiong
Other Information	The best way to communicate with me (other than meeting me in my office during the office hours) is through UTD email. Use email to set up appointments outside the office hours.

General Course Information

Pre-requisites, Co-requisites, & other restrictions	Pre-requisites: CE 2310 or EE 2310 or CS 3340 or SE 3340 or TE 3340 PHYS 2326 Co-requisite: CS 4141/TE 4141
Course Description	Fundamentals of real-time operating systems. Construction and organization. Specific constructs, functions, and services. Processes, threads, communication, synchronization, etc. Design and development of applications in a realistic RTOS environment.
Learning Outcomes	After successful completion of this course, the student should have: 1. Ability to analyze, minimize and design gate-level combinational logic circuits using Boolean algebra and 3 and 4 variable Karnaugh Maps. 2. Ability to analyze and design simple synchronous sequential circuits 3. Ability to analyze, design and utilize digital logic components such as adders, multiplexers, decoders, registers, and counters. 4. Ability to understand RAM and ROM memory components, and utilize these in digital logic design 5. Ability to design computer components such as Arithmetic-Logic-Unit (ALU) and data path 6. Ability to understand the basics of hardware description languages such as Verilog or VHDL.
Required Texts & Materials	**REQUIRED TEXTBOOK:** Digital Design – A System Approach (2012), Dally & Harting, Cambridge University Press, ISBN: 9780521199506. **SUGGESTED TEXTBOOK:** Computer Organization and Design, Fifth Edition, by David A. Patterson & John L. Hennessy, Morgan Kaufmann, 2014. ISBN: 978-0-12-407726-3. **RECOMMENDED READING**: Exploring Digital Logic with Logisim, First Edition, by George Self.

	SUGGESTED READING: Logic and Computer Design Fundamentals, Fourth Edition, by M. Morris Mano and Charles Kime, Prentice Hall, 2007. ISBN: 978-0-13-198926-9. **OTHER MATERIALS:** Other materials including the syllabus, assignments, slides, the publication describing Logisim, etc. will be posted on eLearning. https://elearning.utdallas.edu We will be using a software application called Logisim as an aid to learning about digital logic circuits. Logisim is available for download free at: http://www.cburch.com/logisim/index.html

Assignments & Academic Calendar

Week	Dates	Reading Materials	CLO	Homework Mondays	Programs Wednesdays	Exams On Wednesdays
1	9, 11 Jan	Introduction				
2	18 Jan	Verilog	6		1	
3	23, 25 Jan	Chapters 1, 3, & 6; Appendix A	1	1		
4	30 Jan, 1 Feb	Chapters 7, 8 & 9	3, 4		2	
5	6, 8 Feb	Chapters 10 & 11		2		Exam1
6	13, 15 Feb	Chapter 14	2			
7	20, 22 Feb	Chapter 16		3	3	
8	27 Feb, 1 Mar	Chapter 17				
9	6, 8 Mar	Chapter 18	5	4	4	
	20, 22 Mar	Chapters 20, 21 & 22				Exam2
10	27, 29 Mar	Chapter 23		5	5	
11	3, 5 Apr	Chapter 15				
12	10, 12 Apr	Chapters 27 & 28		6	6	
13	17, 19 Apr					
14	24, 26 Apr	Chapters 22, 24 & 25		7		Exam3
15	TBD					Project

Important Dates and Times	First day of class: Monday, 11 Jan 2016 Exam1: 8 Feb 2016 Exam2: 22 Mar 2016 Exam3: 26 Apr 2016 Project: TBD

Course Policies

Grading Criteria	Exams: 30%, Programs: 30%, Project: 20%, Homework: 10%, Participation: 10%. To pass the course, you must achieve an average of 60 or more on the exams.
Make-up Exams	Make-ups will be offered only if the student has a valid medical reason and produces a doctor's letter (in English) for the specific date. Blanket letters will not be accepted.
Extra Credit	Up to 4 points on final grade for a functional pipelined implementation with a good report. If the code is not fully functional, no points will be granted.
Late Work	Programs and homework submitted after the due date will be penalized at the rate of 10% for every day by which it is late. Late submissions will not be accepted after four days.
Grade Disputes	Grade disputes must be made within two weeks of posting. After that, grades are final.
Class Attendance	Regular attendance is recommended (see participation). By departmental policy, three absences in a row will result in a full letter grade reduction in the final grade. Four absences in a row will result in failing the class. A student absent five or more classes not be eligible for an incomplete grade. In such instances the student is advised to drop the course.
Participation	Participation is an in-class activity related to the discussions in which the student is involved. An anonymous student is one who does not participate. The participation grade is proportional to attendance.
Classroom Citizenship	The instructor encourages students to take active part in class discussions. No question is too simple/stupid to be asked. So, do not hesitate.
Instructor Expectations	Students will: a. Be on time to lectures. b. Be attentive to lectures. c. Be respectful of other's need to avoid distractions. d. Perform their own work unless directed to participate in a group activity. e. Avoid the use of any premade works of answers (the use of which constitutes cheating). f. All student work done outside the classroom will be typewritten.
UT Dallas Syllabus Policies and Procedures	*The information contained in the following link constitutes the University's policies and procedures segment of the course syllabus.* *Please go to http://go.utdallas.edu/syllabus-policies for these policies.*

These descriptions and timelines are subject to change at the discretion of the Professor.