CE/EE 3120.00X Course Syllabus

Course Number/Section CE/EE 3120.00x
Course Title Digital Circuits Laboratory
Term 2017 Spring

Days & Times

Students are not allowed to go to the sections you have not registered without permission, which may induce extra burden to the other sections, and impact the lab resource and TA time for those sections.

If you have special reasons and cannot go to your section, you need to confirm with both TAs for the section you registered and the section you want to go. If you get permission, then you can go to another section for one time. Next time, you still need to get permission.

Please note that, your status will only be recorded by the TA of your registered section. The TA for the section you have not registered will not record your status. So you still need to submit the pre-lab report and show lab results to the TA of your registered section, when you return to your section in the next experiment.

17S Open	EE 3120.101 22115	Digital Circuits Laboratory (1 Credit)	Dian Zhou	Mon : 10:00am-12:45pm ECSN 3.112 Mon : 10:00am-12:45pm ECSN 3.114		View Class Detail Save Class View Textbooks Instructor CV Submit Documents
17S Open	EE 3120.102 22116	Digital Circuits Laboratory (1 Credit)	Dian Zhou	Thurs : 4:00pm-6:45pm ECSN 3.108 Thurs : 4:00pm-6:45pm ECSN 3.110		View Class Detail Save Class View Textbooks Instructor CV Submit Documents
17S Open	EE 3120.103 22117	Digital Circuits Laboratory (1 Credit)	Dian Zhou	Wed : 1:00pm-3:45pm ECSN 3.112 Wed : 1:00pm-3:45pm ECSN 3.114		View Class Detail Save Class View Textbooks Instructor CV Submit Documents
17S Open	EE 3120.104 22118	Digital Circuits Laboratory (1 Credit)	Dian Zhou	Mon : 1:00pm-3:45pm ECSN 3.112 Mon : 1:00pm-3:45pm ECSN 3.114		View Class Detail Save Class View Textbooks Instructor CV Submit Documents
17S Open	EE 3120.105 22119	Digital Circuits Laboratory (1 Credit)	Dian Zhou	Mon : 10:00am-12:45pm ECSN 3.118 Mon : 10:00am-12:45pm ECSN 3.120		View Class Detail Save Class View Textbooks Instructor CV Submit Documents
17S Open	EE 3120.106 22120	Digital Circuits Laboratory (1 Credit)	Dian Zhou	Mon : 1:00pm-3:45pm ECSN 3.108 Mon : 1:00pm-3:45pm ECSN 3.110		View Class Detail Save Class View Textbooks Instructor CV Submit Documents
17S Open	EE 3120.107 27084	Digital Circuits Laboratory (1 Credit)	Dian Zhou	Thurs : 4:00pm-6:45pm ECSN 3.118 Thurs : 4:00pm-6:45pm ECSN 3.120		View Class Detail Save Class Instructor CV Submit Documents

Professor Contact Information

Professor	Dian Zhou
Email Address	zhoud@utdallas.edu
Office Location	ECSN 4.610
Office Hours	By appointment

TA Information

Section 101: Zhaori Bi	zxb107020@utdallas.edu
Section 102: Jiu Xiong	jxx130530@utdallas.edu
Section 103: Qingxue Zhang	qingxue.zhang@utdallas.edu
Section 104: Qingxue Zhang	qingxue.zhang@utdallas.edu
Section 105: Jiu Xiong	jxx130530@utdallas.edu
Section 106: Sameer Arora	sxa093620@utdallas.edu
Section 107: Gaurav Rajavendra Reddy	gxr141930@utdallas.edu
Jiajia Wang	jxw143630@utdallas.edu.

Course Pre-requisites, Co-requisites, and/or Other Restrictions

Prerequisite:	CE/EE 2310 (Digital Systems)
Co-requisites:	CE/EE 3320

Course Description

Designing, assembling and testing of combinational and sequential logic circuits. Logic designs will be done using sample computer-aided design (CAD) tools and implemented using Field Programmable Gate Arrays (FPGAs). In this laboratory digital circuits will be designed and implemented using the Foundation Series Tools and FPGAs from Xilinx, Inc.

Student Learning Objectives/Outcomes

1. Ability to design, assemble, simulate, and test combinational logic design using FPGAs
2. Ability to design, assemble, simulate, and test logic which involves hierarchy
3. Ability to design, assemble, simulate, and test sequential logic design flip-flops and registers.
4. Ability to design, assemble, simulate, and test digital circuits using Verilog.

Required Textbooks and Materials

Required Texts: None
Suggested Course Materials: None

Assignments & Academic Calendar

First class starts from Jan-23-2017.

Week	From	To	Topic	Prelab report	Simulation and Board test results in the lab	Postlab report for lab1
1	1/23/2017	1/29/2017	Lab 0 (redo the video demo)	NA	NA	NA
2	1/30/2017	2/5/2017	Lab 1	lab 1 due	NA	NA
3	2/6/2017	2/12/2017	Lab 1	NA	lab 1 due	NA
4	2/13/2017	2/19/2017	Lab 2	lab 2 due	NA	lab 1 due
5	2/20/2017	2/26/2017	Lab 2	NA	lab 2 due	NA
6	2/27/2017	3/5/2017	Lab 3	lab 3 due	NA	NA
7	3/6/2017	3/12/2017	Lab 3	NA	lab 3 due	NA
8	3/13/2017	3/19/2017	break			
9	3/20/2017	3/26/2017	Lab 4	lab 4 due	NA	NA
10	3/27/2017	4/2/2017	Lab 4	NA	lab 4 due	NA
11	4/3/2017	4/9/2017	Lab 5	lab 5 due	NA	NA
12	4/10/2017	4/16/2017	Lab 5	NA	lab 5 due	NA
13	4/17/2017	4/23/2017	Makeup	submit makeup report if necessary (only simulation part)		
14	4/24/2017	4/30/2017	Makeup	submit makeup report if necessary (only simulation part)		

- The pre-lab reports and lab works are all done individually.
- There are 5 lab assignments, each including one or more tasks. Two weeks (two lab experiments, i.e., two sessions) of time is allocated for each Lab assignment. You can finish it earlier than the due time.
- For each lab assignment, a printed pre-lab report needs to be submitted. The experiment results (design/simulation/test/etc.) need to be shown to the TA in the lab.
- The pre-lab report for each lab assignment is due at the beginning (10 minutes) of the first lab experiment (session) of that assignment. Pre-lab reports that are late but submitted before the end of the first lab experiment (session) will be penalized 30%. No pre-lab report will be accepted after the first lab experiment (session) of that assignment
- The lab report is only necessary for lab 1, which is due at the beginning (10 minutes) of the first experiment (session) of lab 2. Lab reports that are late but submitted before the end of the first experiment (session) of lab 2 will be penalized 30%. No lab report will be accepted after the first experiment (session) of lab 2.
- The lab results for each lab assignment is due at the end of the second lab experiment (session) for each assignment. Otherwise, the lab results will not be graded.

Grading Policy

- Participation: 15%. (Students are required to be present in the first experiment for each lab assignment, and TA will give a detailed introduction on both the lab task and the knowledge needed for the task. Since we have five lab assignments: lab1-lab5, 3% for each presence in the first experiment of each lab.)
- Lab progress check marks: 75%. (TA will verify pre-lab report, simulation and design in the lab)
- Lab 1 Report: 10%. (Submitted at the beginning of class of lab 2. Only for lab1, not necessary for lab2-lab5).

Grades will be assigned as follows:

90% - 100% A

80% - 89% B

70% - 79% C

60 - 69% D

Below 60% F

Please do not copy Lab., pre-lab reports! You will only cheat yourself, if you do. Please read the UT Dallas policy on scholastic dishonesty in this syllabus.

Course & Instructor Policies

Class Attendance

Class attendance is required and FPGA boards may only be used in class. Simulation may be performed outside of the lab but must be shown to the TA to be given credit

UT Dallas Syllabus Policies and Procedures

The information contained in the following link constitutes the University's policies and procedures segment of the course syllabus.
Please go to http://go.utdallas.edu/syllabus-policies for these policies.
The descriptions and timelines contained in this syllabus are subject to change at the discretion of the Professor

Student Conduct & Discipline

The University of Texas System and The University of Texas at Dallas have rules and regulations for the orderly and efficient conduct of their business. It is the responsibility of each student and each student organization to be knowledgeable about the rules and regulations which govern student conduct and activities. General information on student conduct and discipline is contained in the UTD publication, A to Z Guide, which is provided to all registered students each academic year.

The University of Texas at Dallas administers student discipline within the procedures of recognized and established due process. Procedures are defined and described in the Rules and Regulations, Board of Regents, The University of Texas System, Part 1, Chapter VI, Section 3, and in Title V, Rules on Student Services and Activities of the university's Handbook of Operating Procedures. Copies of these rules and regulations are available to students in the Office of the Dean of Students, where staff members are available to assist students in interpreting the rules and regulations (SU 1.602, 972/883-6391).

A student at the university neither loses the rights nor escapes the responsibilities of citizenship. He or she is expected to obey federal, state, and local laws as well as the Regents' Rules, university regulations, and administrative rules. Students are subject to discipline for violating the standards of conduct whether such conduct takes place on or off campus, or whether civil or criminal penalties are also imposed for such conduct.

Academic Integrity

The faculty expects from its students a high level of responsibility and academic honesty. Because the value of an academic degree depends upon the absolute integrity of the work done by the student for that degree, it is imperative that a student demonstrate a high standard of individual honor in his or her scholastic work.

Scholastic dishonesty includes, but is not limited to, statements, acts or omissions related to applications for enrollment or the award of a degree, and/or the submission as one's own work or material that is not one's own. As a general rule, scholastic dishonesty involves one of the following acts: cheating, plagiarism, collusion and/or falsifying academic records. Students suspected of academic dishonesty are subject to disciplinary proceedings.

Plagiarism, especially from the web, from portions of papers for other classes, and from any other source is unacceptable and will be dealt with under the university's policy on plagiarism (see general catalog for details). This course will use the resources of turnitin.com, which searches the web for possible plagiarism and is over 90% effective.

Email Use

The University of Texas at Dallas recognizes the value and efficiency of communication between faculty/staff and students through electronic mail. At the same time, email raises some issues concerning security and the identity of each individual in an email exchange. The university encourages all official student email correspondence be sent only to a student's U.T. Dallas email address and that faculty and staff consider email from students official only if it originates from a UTD student account. This allows the university to maintain a high degree of confidence in the identity of all individual corresponding and the security of the transmitted information. UTD furnishes each student with a free email account that is to be used in all communication with university personnel. The Department of Information Resources at U.T. Dallas provides a method for students to have their U.T. Dallas mail forwarded to other accounts.

Withdrawal from Class

The administration of this institution has set deadlines for withdrawal of any college-level courses. These dates and times are published in that semester's course catalog. Administration procedures must be followed. It is the student's responsibility to handle withdrawal requirements from any class. In other words, I cannot drop or withdraw any student. You must do the proper paperwork to ensure that you will not receive a final grade of "F" in a course if you choose not to attend the class once you are enrolled.

Off-Campus Instruction and Course Activities

Off-campus, out-of-state, and foreign instruction and activities are subject to state law and University policies and procedures regarding travel and risk-related activities. Information regarding these rules and regulations may be

found at the website address given below. Additional information is available from the office of the school dean. (http://www.utdallas.edu/BusinessAffairs/Travel_Risk_Activities.htm)

These descriptions and timelines are subject to change at the discretion of the Professor.