# CE/EE 4304.502 Course Syllabus

**Course Information** 

Course Number/Section CE/EE 4304.502
Course Title Computer Architecture

Term 2016 Fall

Days & Times Tu & Thur: 5:30pm-6:45pm

Meeting Place FN 2.106

**Professor Contact Information** 

Professor William P. Swartz, Jr., Ph.D. Email Address bill-swartz@utdallas.edu

Office Location ECSN 3.610

Office Hours Monday/Wed 4 – 5:30 PM and by appointment

Course Pre-requisites, Co-requisites, and/or Other Restrictions

Prerequisite: CE/EE 3320 (Digital Circuits)

# **Course Description**

Introduction to computer organization and design, including the following topics: CPU performance analysis. Instruction set design, illustrated by the MIPS instruction set architecture. Systems-level view of computer arithmetic. Design of the datapath and control for a simple processor. Pipelining. Hierarchical memory. I/O systems. I/O performance analysis. Multiprocessing.

## **Student Learning Objectives/Outcomes**

The following are the course learning objectives:

- **C001** Understand, and be able to work with, instruction set architectures and the hardware/software interface.
- C002 Understand, and be able to work with, computer arithmetic
- **C003** Understand, and be able to work with, processor architectures.
- C004 Understand, and be able to work with, hierarchical memory architectures.
- C005 Understand, and be able to work with, multiprocessing architectures.

# **Required Textbooks and Materials**

None

# **Suggested Course Materials**

David A. Patterson and John L. Hennessy, *Computer Organization and Design: The Hardware / Software Interface*, Fourth Edition, Revised Printing (Morgan Kaufmann, 2011); ISBN 978-0-12- 374750-1. Any edition is ok. The second edition (out of print) is best.

# **Assignments & Academic Calendar**

Topics covered in the class include but not limited to:

- History
- o Performance Measures
- Amdahl's Law
- o Representations
- Processor Design
  - Single cycle
  - Multi cycle
  - Pipeline
  - Out-of-Order
- Hierarchical Memory
- Multiprocessor Systems

# Homework Due Dates, Exam Dates

Homework will be due at the beginning of class unless otherwise announced via eLearning.

Video quizzes: Announced via eLearning

Midterms: Tue Oct 11, and Tue Nov 8, during class hours (tentatively)

Final examination: TBD

## **Grading Policy**

Homework/Projects: 20%

Quizzes: 10% Midterms: 30%

Final examination: 40% (cumulative)

#### **Course & Instructor Policies**

## Make-up exams

Only by permission of the instructor BEFORE the regularly scheduled examination date *Extra Credit* 

Available for class participation especially at the whiteboard.

#### Late Work

Homework assignments will be considered late at 11:30 PM the Friday after they are due, and will not be graded without a valid excuse.

# Class Attendance

Class attendance is not required. However, material presented in class will substantially augment the optional reading material in the text.

#### Rules for examinations

- 1. Seating is assigned randomly for each exam.
- 2. No materials except for writing instruments are allowed except for the last 10 minutes of the exam. A double-sided 8.5" x 11" sheet of formula cheat sheet will be allowed the last 10 minutes of the exam. Other materials such as books, notebooks and backpacks must be stowed away.
- 3. No calculators or electronic communication devices are allowed.
- 4. No questions are allowed during an examination. If you do not understand the statement of a problem, please state the problem that you think is meant, and solve it.

#### Comet Creed

This creed was voted on by the UT Dallas student body in 2014. It is a standard that Comets choose to live by and encourage others to do the same:

"As a Comet, I pledge honesty, integrity, and service in all that I do."

# **UT Dallas Syllabus Policies and Procedures**

The information contained in the following link constitutes the University's policies and procedures segment of the course syllabus.

Please go to  $\underline{\text{http://go.utdallas.edu/syllabus-policies}} \text{ for these policies.}$ 

The descriptions and timelines contained in this syllabus are subject to change at the discretion of the Professor.