**THE UNIVERSITY OF TEXAS AT DALLAS**
Erik Jonsson School of Engineering and Computer Science
Department of Electrical Engineering

# EEDG/CE 6301: Advanced Digital Logic

(Fall 2016, Tuesday and Thursday: 2:30–3:45 p.m., ECSS 2.410)

## 1 General Information

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|---|---|
| *Instructor:* | Mehrdad Nourani |
| *Office & Phone:* | ECSN 4.924, 972-883-4391 |
| *E-mail (Webpage):* | nourani@utdallas.edu (http://www.utdallas.edu/~nourani) |
| *Office Hours:* | Tuesday 12:30–1:30 p.m. and Thursday 1:00–2:00 p.m., or by appointment. |
| *Recommended Text:* | * *H: Digital Logic Design*, Brian Holdsworth and Clive Woods, Newnes Pub. (Elsevier Science), 2002.<br>* *J: Testing of Digital Systems*, Niraj Jha and Sandeep Gupta, Cambridge University Press, 2003.<br>* *D: Synthesis and Optimization of Digital Circuits*, Giovanni DeMicheli, McGraw Hill 1994. |
| *Other References:* | * *M: Logic Design Principles*, Edward McCluskey, Prentice Hall 1986.<br>* *Computer Aided Logical Design with Emphasis on VLSI*, Frederick Hill and Gerald Peterson, John Wiley 1993.<br>* *Logic Synthesis*, S. Devadas, A. Ghosh and K. Keutzer, McGraw Hill, 1994. |
| *Course Web Page:* | http://elearning.utdallas.edu/ |
| *Teaching Assistant:* | To be announced. |

## 2 Catalog Description

**EEDG/CE 6301 Advanced Digital Logic (3 semester hours).**
Modern design techniques for digital logic. Logic synthesis and design methodology. Link between front-end and back-end design flows. Field programmable gate arrays and reconfigurable digital systems. Introduction to testing, simulation, fault diagnosis and design for testability.
Prerequisite: EE 3320 or equivalent and background in VHDL/Verilog. (3-0) T

## 3 Course Learning Objective

The objective of this graduate level course is to introduce the modern design methodologies for digital logic and automatic synthesis of digital systems. We provide students with access to the CAD tools to use hardware description language to model, analyze and design various digital circuits/systems. It is expected that the students will acquire a clear understanding of the main techniques, design strategies and the optimizations that are involved in modern digital circuit modeling, design and synthesis. In particular, the following are the course learning objectives:

- **CLO1**: Understand the role of optimization and ability to apply multi-output and multi-level optimizations in digital circuit design.
- **CLO2**: Ability to design asynchronous sequential circuits using systematic approaches.
- **CLO3**: Understand the basic process of VLSI testing, stuck-at fault model, fault simulation and the concept of design-for-test methodologies (scan and built-in self-test).
- **CLO4**: Ability to understand and apply graph-based algorithms and linear programming for scheduling, binding and resource sharing in high-level synthesis.
- **CLO5**: Use VHDL/Verilog and CAD tools for optimization, simulation and synthesis.

## 4 Grading

Grading will be based on two tests and homeworks/projects as follows:

| | | |
|---|---|---|
| HWs/Projects: | 20% | |
| Test 1: | 20% | (Tues . 09/13/2016, 2:30 p.m.) |
| Test 2: | 20% | (Thurs. 10/06/2016, 2:30 p.m.) |
| Test 3: | 20% | (Tues. 11/01/2016, 2:30 p.m.) |
| Test 4: | 20% | (Tues. 12/06/2016, 2:30 p.m.) |

| | | |
|---|---|---|
| $85 \leq A- < 93$ | $93 \leq A \leq 100$ | |
| $70 \leq B- < 75$ | $75 \leq B < 80$ | $80 \leq B+ < 85$ |
| $60 \leq C < 65$ | $65 \leq C+ < 70$ | |
| $0 \leq F < 60$ | | |

**Note:** For M.S. degrees, a minimum grade of $B-$ in each and a minimum GPA of 3.0 for all "core" courses are required.

## 5 Course Policies

- Homeworks will be assigned throughout the semester, and will be due approximately once every two weeks at 2:30 p.m. at the **beginning** of the lecture period. Homeworks cannot be submitted by email or fax.
- A homework is considered **late** if it is turned in after 2:30 p.m. of the due date. There will be 20% per day penalty for late homeworks up to 3 days excluding weekends and holidays. Late homeworks and reports won't be accepted after 3 days.
- No makeup examinations/Quizzes/homeworks will be offered in this course. Any graded work can be disputed in writing within one week of the return of that work. In such cases, the entire work will be regraded.

- Some of the homeworks are mini-projects and require C-programming or using CAD tools for implementation, simulation and analysis. These tools are available on almost all Unix machines in ECSN building such as Solarium Lab (ECSN 4.324) and through remote login (e.g. using NX Client or Xmanager) on machines in the ECS open lab (ECSS2.104). To have enough time start as early as possible.
- Copying on examinations, assignments and projects is cheating and is prohibited. Any instances of cheating or plagiarism is considered academic dishonesty and will be subject to disciplinary penalties according to the UT Dallas policy on scholastic dishonesty. The penalties include the possibility of failure in the course and/or dismissal from the University. Since such dishonesty harms the individual, all students and the integrity of the University, policies on scholastic dishonesty will be strictly enforced. Please read carefully this policy in **http://www.utdallas.edu/deanofstudents/dishonesty/**.
- There is no make-up test or homework in this course. Under exceptional circumstances (e.g. hospitalization), official documentation is required and the University policies and procedures will be followed.
- If a student has to be absent for several classes because of job related obligations, (s)he will not be eligible for an incomplete grade. In such cases, the student is advised to withdraw the course.
- Announcements and complementary materials will be posted on the course web page. However, regular attendance and taking notes are highly recommended.

# 6 Syllabus & Tentative Lecture Plan

| *Weeks* | | *Readings* | *Topics Coverage* |
|---|---|---|---|
| *Tue.* | *Thur.* | | |
| 8/23 | | | Introduction: course introduction; technologies and style; |
| | 8/25 | H:Ch 2 | logic-level optimization and synthesis. |
| 8/30 | | H:Ch 3 | Review: logic design; boolean algebra; |
| | 9/1 | | single output and two-level simplification. |
| 9/6 | | H:Ch 3 | Combinational logic: multi-output optimization; |
| | 9/8 | M:Ch 6 | multi-level optimization; Quine-McCluskey algo.; Petrick's method. |
| 9/13 | | | **TEST 1** |
| | 9/15 | H:Ch 8 | VLSI realization; implementation of logic elements; Sequential logic: review of design techniques; |
| 9/20 | | H:Ch 8 | design of clock-mode (synchronous) sequential circuit; case studies |
| | 9/22 | H:Ch 9 | design of level-mode (asynchronous) sequential circuit; |
| 9/27 | | H:Ch 9 | optimization of asynchronous sequential systems; case studies. |
| | 9/29 | | issues of asynchronous circuit design. |
| 10/4 | | H:Ch 9 | Programmable logic devices: PLD, PGA, PLA, PAL; case studies; |
| | 10/6 | H:Ch 11 | **TEST 2** |
| 10/11 | | J:Ch 2 | VLSI Testing: design for testability; fault models; boolean difference; |
| | 10/13 | J:Ch 4 | test generation algorithms; fault simulation; |
| 10/18 | | J:Ch 11 | built-in-self test; scan-path methods; boundary scan standard. |
| | 10/20 | | Design Automation: y-chart; hardware modeling; high-level synthesis. |
| 10/25 | | D:Ch 1 | Fundamental Algorithms: graph theory background; |
| | 10/27 | D:Ch 2 | algorithms for synthesis; Branch&Bound; greedy; LP/ILP; graph-based algorithms. |
| 11/1 | | D:Ch 4 | **TEST 3** |
| | 11/3 | | Scheduling: main strategies and tradeoffs; scheduling under resource |
| 11/8 | | D:Ch 5 | and time constraints; list scheduling; force-directed scheduling; |
| | 11/10 | | Binding: resource sharing; clique-based algorithm; |
| 11/15 | | D:Ch 6 | ILP model for binding; left-edge algorithm; |
| | 11/17 | | register sharing; MUX/BUS sharing; module selection; Datapath/Controller Generation. |
| 11/22 | | | **Fall Break & Thanksgiving – University Holiday** |
| | 11/24 | | |
| 11/29 | | literature | Miscellaneous Topic: concurrent scheduling and binding; |
| | 12/1 | | low power digital design; core-based SoC design; |
| 12/6 | | | **TEST 4** |

**Note:** Some topics in this course syllabus are not fully covered in any text book.

# 7 Comet Creed

This creed was voted on by the UT Dallas student body in 2014. It is a standard that Comets choose to live by and encourage others to do the same: **"As a Comet, I pledge honesty, integrity, and service in all that I do."**

# 8 UT Dallas Syllabus Policies and Procedures

The information contained in the following link constitutes the University's policies and procedures segment of the course syllabus. Please go to **http://go.utdallas.edu/syllabus-policies** for these policies.