UTD

Course	**EE 4330: Integrated Circuit Technology**
Instructor	Chadwin D. Young
Term	Fall 2016
Meetings	Location: SLC 2.302 Mondays & Wednesdays: 2:30 AM – 3:45 PM

Professor's Contact Information

Office Phone	972-883-5770
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Office Hours	Monday 1:00 – 2:00 AM or by appointment
Other Information	Best contact is through email

General Course Information

Course Description	Principles of design and fabrication of integrated circuits. Bipolar and MOS technologies. Passive and active component performance, fabrication techniques including epitaxial growth, photolithography, oxidation, diffusion, ion-implantation, thin and thick film components. Design and layout of integrated devices. Relations between layout and fabrication technique. Prerequisite: CE 3310 or EE 3310. (3-0)
Course Learning Outcomes	1. Ability to evaluate and analyze concepts in lithography, etch, and fabrication flow 2. Ability to evaluate and analyze concepts in surface modification: doping and oxidation. 3. Ability to evaluate and analyze concepts in film deposition, interconnections, contacts, packaging 4. Ability to evaluate and analyze concepts in the integration of processes to make MOS or bipolar devices
Syllabus	• Overview of IC Technology • Silicon Substrates • Epitaxial Growth • Oxidation • Photolithography • Etching • Diffusion • Ion Implantation • Rapid Thermal Processing • Thin Film Deposition • Process Integration, Design and Layout • Packaging and Yield • Current Research/Topics
Suggested Texts, Readings, & Materials	1. *Fabrication Engineering at the Micro and Nanoscale* by Stephen A. Campbell (ISBN: 9780199861224) 2. *Introduction to Microelectronic Fabrication* by Richard C. Jaeger, Prentice Hall, 2002. 3. *Silicon VLSI Technology* by J. Plummer, M. Deal, and P. Griffin, Prentice Hall, 2000.
UT Dallas Syllabus Policies and Procedures	*The information contained in the following link constitutes the University's policies and procedures segment of the course syllabus.* *Please go to http://go.utdallas.edu/syllabus-policies for these policies.*