Course Syllabus

Course Information

CS/TE 4341.0U1 – Digital Logic and Computer Design

Term : Summer 2016
Days & Time and Location : MW 3:00PM-5:15PM @ ECSS 2.203

Instructor Contact Information

Nhut Nguyen, Ph.D.
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Office hours: MW 2:00PM – 3:00PM,
also by appointment
Office: *ECSS 3.607*

Course Pre-requisites, Co-requisites, and/or Other Restrictions

EE 2310: Introduction to Digital Systems or CS 3340: Computer Architecture, and PHYS 2326: Electromagnetism and Waves. Students that have completed CS 4340 cannot get credit for this course.
Co requisite: CS 4141: Digital Systems Laboratory (1 semester hour) Laboratory to accompany CS 4341. The purpose of this laboratory is to give students an intuitive understanding of digital circuits and systems. Laboratory exercises include construction of simple digital logic circuits using prototyping kits and board-level assembly of a personal computer. Students that have credit for CS 2110 have credit for this course and cannot get additional credit for this course t.

Course Description

CS 4341: Digital Logic and Computer Design (3 semester hours)
This course focuses on topics required for hardware design of computer systems. Topics include Boolean algebra and logic circuits; combinational and synchronous sequential circuits; gate level design of digital building blocks, registers, and memory unit; register transfer operations; design of data path and control unit for a small computer; memory system, Input-Output (I/O) interfaces.

Students that have completed CS 4340 cannot get credit for this course.

Student Learning Objectives/Outcomes

The main objective of this course is to study topics leading to the understanding and ability to design a computer using digital logic circuits, starting from basic gates and elementary Boolean algebra.

After successful completion of this course, the student should have

- Ability to analyze, minimize and design gate-level combinational logic circuits using Boolean algebra and 3 and 4 variable Karnaugh Maps.
- Ability to analyze and design simple synchronous sequential circuits
- Ability to analyze, design and utilize digital logic components such as adders, multiplexers, decoders, registers, and counters.
- Ability to understand RAM and ROM memory components, and utilize these in digital logic design
- Ability to design computer components such as Arithmetic-Logic-Unit (ALU) and data path
- Ability to understand the basics of hardware description languages such as Verilog or VHDL.

Required Textbook:

"Digital Design – a system approach" (2012),
Dally & Harting, Cambridge University Press, ISBN: 9780521199506.

Reference:
"Digital Design and Computer Architecture" Second edition (2013),
Harris & Harris, Morgan Kauffman, ISBN: 978-0-12-394424-5.

Required Course Materials: To be discussed and provided in class.

Assignments & Academic Calendar

Exams: There will be two exams during the course, and the second exam is comprehensive. Exam materials will be taken mainly from classroom lectures and require a clear understanding of topics discussed in class.

Assignments: There will be regularly assigned reading and homework. Reading assignments should be done before the class session.

Project: A team project may be assigned. Details will be announced in class.

Tentative Class Schedule

Session	*Date*	*Topic*	*Reading Assignment*	*Assignments*	*Due*
1	May 23	Introduction The digital abstraction - 1	Ch 1.1-3		
2	May 25	The digital abstraction – 2 Verilog	Ch 7.1, App-A	HW #1	
3	June 1	Boolean algebra			
4	June 6	Combinational logic design -1	Ch 6.1-9		HW #1
5	June 8	Combinational logic design -2	Ch 7	HW#2	
6	June 13	Combinational building blocks -1	Ch 8		
7	June 15	Combinational building blocks – 2	Ch 9		HW#2
8	June 20	Numbers and arithmetic	Ch 10	HW #3	
9	June 22	Sequential logic design – FSM 1	Ch 14		
10	June 27	Sequential logic design – FSM 2	Ch 5.3-5		HW #3
11	June 29	**Exam I**			
12	July 6	Sequential building blocks & FSM factoring	Ch 16-17	HW #4	
13	July 11	Data path & Control			
14	July 13	Timing	Ch 15		HW #4
15	July 18	Microcode	Ch 18	HW #5	
16	July 20	System design	Ch 21		
17	July 25	Pipelining	Ch 23		HW #5
18	July 27	Sequential logic review	Ch 27, 28	HW #6	
19	Aug 1	System topics	Ch 22, 24, 25		
20	Aug 3	Exam II review			HW #6
21	Aug 8	**Exam II**			

Grading Policy

The grade each student earns from this class will be based on the following table:

Exam I	15%
Exam II	40%
Project	25%
Assignments	20%
Total	100%

Grades are assigned according to the scale on the right:

A	93.0 - 100
A-	90.0 - 92.9
B+	87.0 - 89.9
B	83.0 - 86.9
B-	80.0 - 82.9
C+	77.0 - 79.9
C	73.0 - 76.9
C-	70.0 - 72.9
D+	67.0 - 69.9
D	60.0 - 66.9
F	Below 60.0

Course & Instructor Policies

There will be no makeup exams under normal circumstances.
No late homework or assignment will be accepted!

UT Dallas Syllabus Policies and Procedures

The information contained in the following link constitutes the University's policies and procedures segment of the course syllabus.

Please go to *http://go.utdallas.edu/syllabus-policies* for these policies.

These descriptions and timelines are subject to change at the discretion of the Instructor.