Course Syllabus

Course Information

CS/SE/TE 3340.0U1 – Computer Architecture

Term : Summer 2016
Days & Time and Location : MW 10:00AM-12:15PM @ ECSS 2.201

Instructor Contact Information

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Course Pre-requisites, Co-requisites, and/or Other Restrictions
CE/CS/TE 1337 or equivalent, and CE/CS/TE 2305 or equivalent.

Course Description

This course introduces the concepts of computer architecture by going through multiple levels of abstraction, the representation of data (e.g. numbers) and instructions in memory. It focuses on the instruction-set architecture (ISA) of the MIPS machine, including MIPS assembly language, translation between MIPS and C, and between MIPS and machine code. General topics include processor performance calculation, processor datapath, pipelining, and memory hierarchy. Students that have credit for CS 2310 or CS/SE4340 cannot receive credit for this course (3 semester hours).

Student Learning Objectives/Outcomes

After successful completion of this course, the student should

1. be able to write a functional, stand-alone medium size assembly language program (e.g. a basic Telnet client.)
2. have an ability to represent numbers in and convert between decimal, binary, and hexadecimal and perform calculations using 2's complement arithmetic.
3. understand the basic model of a computer including the datapath, control, memory, and I/O components.

4. be able to program efficiently in an assembly level instruction set, including the use of addressing modes and data types.
5. understand the role of compilers, assemblers, and linkers and how programs are translated into machine language and executed.
6. be able to demonstrate comprehension of a pipelined architectures including datapaths and hazards.
7. be able to demonstrate comprehension of computer performance measures and their estimation.
8. understand the memory hierarchy including caches and virtual memory.

Required Textbook:
"Computer Organization and Design - The Hardware/Software Interface – 5th Edition", *Patterson and Hennessey*, Morgan-Kaufmann, 2013. ISBN-13: 978-0124077263. ***Note: there are several editions of the same title, make sure that you get the correct edition (for MIPS***).

Required Course Materials:

RISC ASSEMBLER/SIMULATOR

It is assumed you are familiar with the PC environment, can create and edit text files, run programs, etc. The programs will be in assembly language for the MIPS processor. This course uses the MARS MIPS assembler and simulator. MARS is available, free, for download from the Internet through the site: http://courses.missouristate.edu/kenvollmar/mars/.
The MARS simulator can assemble MIPS assembly language source files, load and run them with a users console window for input/output, and debug them if they do not work properly.

Assignments & Academic Calendar

Exams: There will be two exams during the course and the second exam is comprehensive. Test materials will be taken mainly from classroom lectures and require a clear understanding of topics discussed in class.

Assignments: There will be regularly assigned reading and homework. Reading assignments should be done before the class session. Homework and project will require the student to spend significant amount of time performing MIPS assembly language programming outside of class.

MIPS assembly language programming assignments should be submitted using your eLearning account. Each programming assignment must contain:

1. A copy of the final working assembly language source code with comments and documentation. The file should be "text-only" and the extension must be ".s" or ".asm". Documentation for the program can be a separate text or Word document.
2. A Word document showing your program's keyboard input and displayed output (using a screen capture program such as snipping tool in Windows).

Project: A programming project will be assigned. Details will be announced in the class.

Tentative Class Schedule

Session	Date	Topic	Reading assignment	Assignment	Assignment due
1	May 23	Intro to Computer Organization	Ch 1		
2	May 25	Introduction to Assembly Language programming	Appendix A	HW #1	
3	June 1	Performance Evaluation, Amdahl's Law	Ch 1.6,1.9		HW #1
4	June 6	Data & Instruction Representations I	Ch.2.3		
5	June 8	Data & Instruction Representations II	Ch.2.4-2.5	HW#2	
6	June 13	Comparing, Branching and Looping	Ch 2.2, 2.7		
7	June 15	Bits and bytes manipulation & other instructions	Ch 2.6		HW#2
8	June 20	Integer & Floating Point Arithmetic	Ch 3.1-3.5	HW #3	
9	June 22	Comparing ISAs Exam I Review	2.16-2.17		
10	June 27	**Exam I**			HW #3
11	June 29	Subroutines	Ch 2.8. A.6		
12	July 6	Addressing modes & System software Input & Output	Ch 2.10, 2.12-13	HW #4	
13	July 11	Interrupts and Exceptions	Ch 4.9, A.7		
14	July 13	Processor: Datapath & Control	Ch 4.1-4		HW #4
15	July 18	Processor: Pipelining	Ch 4.5	HW #5	
16	July 20	Processor: Pipelined Datapath	Ch 4.6-8		
17	July 25	Advanced Instruction Level Parallelism	Ch 4.10		HW #5
18	July 27	Introduction to memory hierarchy	Ch 5.1-4		
19	Aug 1	Virtual Memory	Ch 5.7-8		
20	Aug 3	Exam II Review			**Project**
21	Aug 8	**Exam II**			

Grading Policy

The grade each student earns from this class will be based on the following table:

Exam I	15%
Exam II	40%
Project	25%
Homework & quizzes	20%
Total	100%

A	93.0 - 100
A-	90.0 - 92.9
B+	87.0 - 89.9
B	83.0 - 86.9
B-	80.0 - 82.9
C+	77.0 - 79.9
C	73.0 - 76.9
C-	70.0 - 72.9
D+	67.0 - 69.9
D	60.0 - 66.9
F	Below 60.0

Grades are assigned according to the scale on the right:

Programming assignments:

Code Development	30%	(compile w/o error)
Program Execution	20%	(run successfully)
Program Design	25%	(conform to spec)
Documentation	15%	(program, comments)
Coding Style	10%	(clear, efficient)

Course & Instructor Policies

There will be no makeup exams under normal circumstances.
No late homework or assignment will be accepted!

UT Dallas Syllabus Policies and Procedures

The information contained in the following link constitutes the University's policies and procedures segment of the course syllabus.

Please go to *http://go.utdallas.edu/syllabus-policies* for these policies.

These descriptions and timelines are subject to change at the discretion of the Instructor.