

Course CS 4341.003, Digital Logic and Computer Design

Professor Richard Goodrum **Term** Spring 2015

Meetings MW 2:30-3:45 P.M., Room: ECSS 2.415

Professor's Contact Information

Office Phone	TBD			
Other Phone	(972) 883-2185 (CS Department Phone Number)			
Office Location	ECSS 4.403			
Email Address	Richard.Goodrum@utdallas.edu			
Office Hours	8:00 A.M9:45 A.M. Monday through Thursday			
Teaching Assistant	Baoye Xue			
	The best way to communicate with me (other than meeting me in my			
Other Information	office during the office hours) is through UTD email. Use email to set up			
	appointments outside the office hours.			

General Course Information

General Course line					
Pre-requisites, Co-	•				
requisites, & other	PHYS 2326				
restrictions	Co-requisite: CS 4141/TE 4141				
Course Description	Fundamentals of real-time operating systems. Construction and organization. Specific constructs, functions, and services. Processes, threads, communication, synchronization, etc. Design and development of applications in a realistic RTOS environment.				
Learning Outcomes	 After successful completion of this course, the student should have: Ability to analyze, minimize and design gate-level combinational logic circuits using Boolean algebra and 3 and 4 variable Karnaugh Maps. Ability to analyze and design simple synchronous sequential circuits Ability to analyze, design and utilize digital logic components such as adders, multiplexers, decoders, registers, and counters. Ability to understand RAM and ROM memory components, and utilize these in digital logic design Ability to design computer components such as Arithmetic-Logic-Unit (ALU) and data path Ability to understand the basics of hardware description languages such as Verilog or VHDI 				
Required Texts & Materials	as Verilog or VHDL. REQUIRED TEXTBOOK: Digital Design – A System Approach (2012), Dally & Harting, Cambridge University Press, ISBN: 9780521199506. SUGGESTED TEXTBOOK: Computer Organization and Design, Fifth Edition, by David A. Patterson & John L. Hennessy, Morgan Kaufmann, 2014. ISBN: 978-0-12-407726-3. REQUIRED READING (Provided on eLearning): Exploring Digital Logic with Logism, First Edition, by George Self.				

SUGGESTED READING:

Logic and Computer Design Fundamentals, Fourth Edition, by M. Morris Mano and Charles Kime, Prentice Hall, 2007. ISBN: 978-0-13-198926-9.

OTHER MATERIALS:

Other materials including the syllabus, assignments, slides, the publication describing Logism, etc. will be posted on eLearning. https://elearning.utdallas.edu

We will be using a software application called Logisim as an aid to learning about digital logic circuits. Logism is available for download free at: http://www.cburch.com/logisim/index.html

Assignments & Academic Calendar

Week	Class	Dates	Reading Materials	Course	Major
			J	Learning Outcomes	Assignments
1	1, 2	Jan 11, 13	Introduction		
2	3, 4	Jan 18, 20	Holiday, Verilog	6	
3	5, 6	Jan 25, 27	Chapters 1, 3, & 6; Appendix A	1	
4	7, 8	Feb 1, 3	Chapters 7, 8 & 9	3, 4	
5	9, 10	Feb 8, 10	Chapters 10 & 11		
6	11, 12	Feb 15, 17	Chapter 14	2	Exam 1
7	13, 14	Feb 22, 24	Chapter 16		
8	15, 16	Feb 29, Mar 2	Chapter 17		
9	17, 18	Mar 7, 9	Chapter 18	5	
	Spring Break	Mar 14, 16			
10	19, 20	Mar 21, 22	Chapters 20, 21 & 22		
11	21, 22	Mar 28, 30	Chapter 23		
12	23, 24	Apr 4, 6	Chapter 15		
13	25, 26	Apr 11, 13	Chapters 27 & 28		
14	27, 28	Apr 18, 20			
15	29, 30	Apr 25, 27	Chapters 22, 24 & 25		Project
		TBD			Exam 2

	First day of class: Monday, 11 Jan 2016		
Important Dates and	Exam 1:	Thursday, 17 Feb 2016	
Times	Project:	Thursday, 27 Apr 2016	
	Exam 2:	TBD	

Course Policies

Course Policies					
	Exam 1: 20%, Exam 2: 20%, Project: 20%,				
Grading	Programs: 20%, Homework: 10%, Participation: 10%.				
Criteria					
	To pass the course, you must pass each exam and the programming projects.				
Make-up	Make-up examinations will be offered only if the student has a valid medical				
Exams	reason and produces a doctor's letter.				
Extra Credit					
	Programming projects and homework submitted after the due date will be				
	penalized at the rate of 25% of the total credit for that assignment for every				
T 4 TT7 1	day by which it is late. I ate submissions will not be accented once the				
Late Work	solution has been discussed in class or the graded submissions have been				
	returned. All work must be submitted before the end of the final exam period				
	as provided by the Registrar's office.				
	Regular attendance is recommended as it represents 10% of the course grade				
	(participation). If a student has to be absent for three or more classes except				
Class	medical reasons with a doctor's note, the student will not be eligible for an				
Attendance	incomplete grade. If a student is absent more than five times including				
	medical reasons, the student is advised to drop the course.				
Classroom	The instructor encourages students to take active part in class discussions. No				
Citizenship	question is too simple/stupid to be asked. So, do not hesitate.				
Citizensinp	Students will:				
	a. Be on time to lectures.				
	b. Be attentive to lectures.				
	c. Be respectful of other's need to avoid distractions.				
Instructor	d. Perform their own work unless directed to participate in a group				
Expectations	activity.				
	e. Avoid the use of any premade works of answers (the use of which				
	constitutes cheating).				
	f. All student work done outside the classroom will be typewritten.				
Field Trip					
Policies	Not applicable.				
UT Dallas	The information contained in the following link constitutes the University's				
Syllabus	policies and procedures segment of the course syllabus.				
Policies and	I I I I I I I I I I I I I I I I I I I				
Procedures	Please go to http://go.utdallas.edu/syllabus-policies for these policies.				
	and time lines are subject to all many at the discretion of the Druckers				

These descriptions and timelines are subject to change at the discretion of the Professor.