Course Syllabus

Course Information

CS/SE 3340.501 – Computer Architecture

<u>Term</u> : <u>Days & Time and Location</u> : Fall 2013 TTh 5:30PM - 6 :45PM @ ECSS 2.412

Instructor Contact Information

Nhut Nguyen, Ph.D. Phone: 972-883-4521 Email: <u>nhutnn@utdallas.edu</u> Web: <u>www.utdallas.edu/~nhutnn</u> Office hours: TTh 4:00PM – 5:30PM and by appointment Office: *ECSS 3.607*

Course Pre-requisites, Co-requisites, and/or Other Restrictions

CE/CS/TE 1337 or equivalent. CE/CS/TE 2305 or equivalent.

Course Description

This course introduces the concepts of computer architecture by going through multiple levels of abstraction, the numbering systems and their basic computations. It focuses on the instruction-set architecture of the MIPS machine, including MIPS assembly programming, translation between MIPS and C, and between MIPS and machine code. General topics include performance calculation, processor datapath, pipelining, and memory hierarchy. Students that have credit for CS 2310 or CS/SE4340 cannot receive credit for this course (3 semester hours).

Student Learning Objectives/Outcomes

After successful completion of this course, the student should

- be able to write a fully functional, stand-alone medium size assembly language program (e.g. a basic Telnet client)
- have an ability to represent numbers in and convert between decimal, binary, and hexadecimal and perform calculations using 2's complement arithmetic
- understand the basic model of a computer including the datapath, control, memory, and I/O components

- be able to program efficiently in an assembly level instruction set, including the use of addressing modes and data types
- understand the role of compilers, assemblers, and linkers and how programs are translated into machine language and executed
- be able to demonstrate comprehension of a pipelined architectures including datapaths and hazards
- understand the memory hierarchy including caches and virtual memory
- be able to demonstrate comprehension of computer performance measures and their estimation

Required Textbook:

"Computer Organization and Design - The Hardware/Software Interface – REVISED 4th Edition", *Patterson and Hennessey*, Morgan-Kaufmann, 2012. ISBN-13: 978-0123747501. *Note: there are several editions of the same title, make sure that you get the correct edition (for MIPS)*.

Required Course Materials:

RISC ASSEMBLER/SIMULATOR

It is assumed you are familiar with the PC environment, can create and edit text files, run programs, etc. The programs will be in assembly language for the MIPS processor. This course uses the MARS MIPS assembler and simulator. MARS is available, free, for download from the Internet through the site:

http://courses.missouristate.edu/kenvollmar/mars/.

The MARS simulator can assemble MIPS assembly language source files, load and run them with a users console window for input/output, and debug them if they do not work properly. The MIPS R2000 Assembly Language reference is contained in section A.10.

Assignments & Academic Calendar

Exams: There will be three exams during the course: two midterms and a final exam. The exams will be open book, and will be limited to material covered during the immediate unit. Test material will be taken mainly from classroom lectures.

Assignments: There will be regularly assigned reading and homework. Reading assignments should be done before the class session. Homework will require the student to spend time programming a computer outside of class. It includes a program to demonstrate the correct operation of the assigned tasks.

Programming assignments should be submitted using your eLearning account. Each programming assignment must contain:

1. A copy of the final working assembly language source code with comments and documentation. The file should be "text-only" and the extension must be ".s" or ".asm".

2. A copy of your program's keyboard input and displayed output from the console (.txt/.doc).

Project: A team programming project will be assigned. Details will be announced in the class.

Class Schedule

| Session | Date | Торіс | Reading | Assignments | Due |
|---------|--------|--|--------------|-------------|---------|
| 1 | Aug 27 | Introduction | | | |
| 2 | Aug 29 | Intro to computer organization | Ch 1 | | |
| 3 | Sep 03 | Performance evaluation, Amdahl's law | Ch 1.4,1.8 | HW #1 | |
| 4 | Sep 05 | Number representations Bin/Oct/Hex | Ch.2.4 | | |
| 5 | Sep 10 | 1's and 2's complement arithmetic | | | HW #1 |
| 6 | Sep 12 | Instruction Set Architecture (ISA) | | HW #2 | |
| 7 | Sep 17 | Computer arithmetic | Ch 3.1-3.4 | | |
| 8 | Sep 19 | Floating point arithmetic | Ch 3.5 | | HW #2 |
| 9 | Sep 24 | MIPS simulator and I/O support | Appendix B | HW #3 | |
| 10 | Sep 26 | Assembly Ops: Load/Store/Add/Sub/etc | Ch 2.1-2.5 | | |
| 11 | Oct 01 | Comparing, branching and looping | Ch 2.7 | | HW #3 |
| 12 | Oct 03 | Exam I review | Ch 2.8 | HW #4 | |
| 13 | Oct 08 | Exam I | | | |
| 14 | Oct 10 | Procedures: machine language calls | | | HW #4 |
| 15 | Oct 15 | Comparing ISAs: MIPS vs. ARM and x86 | | HW #5 | |
| 16 | Oct 17 | Bits and bytes manipulation & other instructions | Ch 2.6, 2.9, | | |
| 17 | Oct 22 | Addressing modes & system software | 2.12, 2.13 | | HW #5 |
| 18 | Oct 24 | Input & Output | Ch 6.5-8 | HW #6 | |
| 19 | Oct 29 | Interrupts and exceptions | Ch 4.9 | | |
| 20 | Oct 31 | Exam II review | | | HW #6 |
| 21 | Nov 05 | Exam II | | | |
| 22 | Nov 07 | Processor: Datapath & Control | Ch 4.1-4 | HW #7 | |
| 23 | Nov 12 | Processor: pipelining | Ch 4.5 | | |
| 24 | Nov 14 | Processor: pipelined Datapath & Control | Ch 4.6 | | HW #7 |
| 25 | Nov 19 | Processor: Hazards | Ch 4.7-8 | | |
| 26 | Nov 21 | Instruction-Level parallelism | Ch 4.10 | | |
| 27 | Nov 26 | No Class | | | |
| 28 | Nov 28 | No Class | | | |
| 29 | Dec 03 | Introduction to memory hierarchy | Ch 5 | | |
| 30 | Dec 05 | Exam III Review | | | Project |
| 31 | Dec 10 | Exam III | | | |

Grading Policy

The grade each student earns from this class will be based on the following table:

| | | | А | |
|--|------|--|----------|--|
| Exam I | 10% | | A- | |
| Exam II | 20% | | B+ | |
| Exam III | 30% | | В | |
| Assignments and quizzes | 20% | | B- | |
| Project | 20% | | с. С. | |
| Total | 100% | | C+ | |
| | | | С | |
| | | | C- | |
| | | | D+ | |
| Grades are assigned according to the scale on the right: | | | | |
| | | | F | |
| | | | | |

Programming assignments:

| 30% | (compile w/o error) |
|-----|---------------------------------|
| 20% | (run successfully) |
| 25% | (conform to spec) |
| 15% | (program, comments) |
| 10% | (clear, efficient) |
| | 30% 20% 25% 15% 10% |

Course & Instructor Policies

There will be no makeup exams under normal circumstances. No late homework or assignment will be accepted!

UT Dallas Syllabus Policies and Procedures

The information contained in the following link constitutes the University's policies and procedures segment of the course syllabus.

Please go to <u>http://go.utdallas.edu/syllabus-policies</u> for these policies.

These descriptions and timelines are subject to change at the discretion of the Instructor.

93.0 - 100 90.0 - 92.9 87.0 - 89.9 83.0 - 86.9 80.0 - 82.9 77.0 - 79.9 73.0 - 76.9 70.0 - 72.9 67.0 - 69.9 60.0 - 66.9 Below 60.0