EE/CE 3320 DIGITAL CIRCUITS, Fall 2025
Electrical and Computer Engineering
Erik Jonsson School of Engineering & Computer Science at UTD

Professor: Tooraj Nikoubin
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Office Hours: W 12noon-01pm by appointment
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Location: ECSW 3.250
Time: MW 10:00am – 11:15am

Course Description

The importance of digital circuits and systems cannot be overestimated in the present day and age. Digital circuits form the basis for most electronic devices ranging from small electronic toys to large scale computers. Hence it is useful to understand how these circuits are designed and operated. All digital circuits operate using the same concepts that will be presented in this class. The only difference is in the complexity of the circuits.

Course Pre-requisites

Prerequisites: EE 2310

Course Learning Objectives

- Ability to design, analyze, and optimize combinational logic circuits
- Ability to design, analyze, and optimize synchronous sequential logic circuits
- Ability to conduct timing analysis on combinational and sequential logic circuits
- Ability to understand and apply practical aspects of digital design including data path components
- Ability to understand logic gate implementations and their electrical properties

Course Material

- **Required Text Book:**

- Charles H.Roth, Jr. and Larry L. Kinney, "Fundamentals of Logic Design"

- **References:**

- Frank Vahid: *Digital Design –with RTL Design, VHDL, and Verilog,* John Wiley Publishers. Second Edition, ISBN: 978-0-470-53108-2.
- S. Brown and Z. Vranesic, *Fundamentals of Digital Logic with Verilog Design*, McGraw-Hill Publishing. Second Edition, 2008
- All announcements and homework assignments will be posted online for this course. It is the responsibility of each student to check this web page at least once a week for new announcements and homework.

Academic Calendar

- First Class Day: Monday, Aug 25, 2025
- Last Class Day: Tuesday, Dec 16, 2025
- Fall Break: Nov 27th to Nov 30th

- 1st Exam: will be announced one week before exam,
- 2nd Exam: will be announced one week before exam,
- 3rd Exam: Final Exam schedule TBA

● Course Announcements and Homework Assignments

Course announcements and homework assignments will be posted on the web page for this course. Sometimes homework provides practice to solve difficult problems. Students are welcome to discuss homework with the instructor and teaching assistants.

● Grading Policy

Final grades in this course will be based on several homework assignments and two examinations given throughout the semester and a final examination. No makeup examinations will be offered in this course. Any graded work can be disputed in writing *within one week* of the return of that work. Complete work will be re-graded.
The grading policy is:

	Course Requirements and Corresponding Weight	
1	Test # 1	15%
2	Test # 2	15%
3	Final exam	30%
4	Project	10%
5	Homework and Class Activities	30%

● UT Dallas Policies and Procedures

For all issues related to sharing confidential information, student conduct and discipline, academic integrity, student grievance, incomplete grade, and other student related university policies please refer to this page: http://go.utdallas.edu/syllabus-policies

● Course Modality and Expectations

a. Instructional Mode

The mode of instruction will be Traditional Classroom (in-person) in this semester for this class.

b. Course Platform

Please use eLearning for access to the notes, submission of assignments (including HWs, Project report and quizzes), grading, etc. in this course.

c. Expectations

Students are expected to attend all lectures in-person at UTD, to submit all assignments, projects and other course requirement shown in this course on time. Students are expected to conduct professionally in all interactions with the TA and the instructor for the course material and projects. Any violations of the university rules and regulations will be referred to the university committee on student conduct. Please see Student Code of Conduct for more information.

d. Asynchronous Learning Guidelines

There is no asynchronous mode of learning for this course

- **List of Topics (subject to base on the progress of the class)**

No.	Topic	Text Section # [Online Section #]
1	**Introduction**	PPT
2	**Digital Logic Design Fundamentals (Review)** a. *Review*: Truth tables, Boolean algebra and algebraic proofs, AND-OR, OR-AND, NAND, NOR, XOR, XNOR circuits d. Logic minimization (SOP and POS forms) e. Karnaugh Map f. Transistor Level Realization of the logic gates g. Timing analysis of the circuits	PP. 1-12, 36-52, pp. 94-104 pp. 134-153 PPT PPT
3	**Quine-McClusky Method**	pp. 173-184
4	**Multi-level gate circuits** a. AND-OR, OR-AND (AOI & OAI) b. NAND-NAND & NOR-NOR configurations c. Other configurations	pp. 199-217 PPT 206 PPT
5	**Combinational circuit design and simulation** a. Design of the circuit with limited fan-in b. Gate delays and timing diagrams **c.** Hazards in combinational logic	pp. 229-242 229 232 240
6	**Multiplexers, Decoders, and Programable Logic Designs** a. Multiplexers b. Three-state buffers c. Decoders and Encoders d. Read-Only Memories e. Programable Logic devices f. Complex programable logic devices g. Field-Programable Gate Arrays c. Binary Adders and Subractors, d. Comparators	pp. 260-285 261 265 268 271 275 280 282 PPT PPT
7	**Coding** a. BCD, Aiken, Excess 3, Gray, and some other codes b. Code converters (like Decimal to BCD convertor) c. 7-segment display d. Even parity and error detection e. BCD Adder and subtractor	PPT
8	**Combinational logic design using Verilog** a. Even parity and one bit error detection b. Hamming with even parity and one bit error correction (First Project)	(Video Tutorials) PPT PPT
9	**Latches and Flip-Flops, Buffer, shift Register** a. Set-Reset Latch b. Gate Latches c. Edge-Triggered D Flip-Flop d. S-R Flip-Flop e. J-K Flip-Flop f. T Flip-Flop g. Buffer, Shift Register	pp. 331-354 338 342 346 349 350 351 380
10	**Counters and Counter design** a. Design of BCD Counter b. Design of Binary Counter c. Count up and count down counter d. Counter design using D, T, RS and JK Flip-Flops e. Counters for other sequences f. Multistage counters g. Digital watch	 PPT 384 PPT 395 389 PPT PPT

11	**Analysis of clocked sequential circuits** a. Frequency dividers b. Timing analysis of Synchronous circuits c. Timing analysis of Asynchronous circuits d. Sequential logic design using Verilog e. Binary Programable Timer (Second Project) e. Digital watch	**PPT** **PPT** **PPT** **PPT** Video Tutorial **PPT**
12	**Derivation of state Graphs and State Tables (FSM)** a. Design of Sequence Detector d. More complex Design Problems e. Guidelines for Construction of State Graph f. Elimination of Redundant States g. Equivalent states h. Determination of state equivalence using an implication table i. Timing analysis of state machines	453-497 457 463 467 505 507 509 **PPT**
13	**Advanced Topics** • FSM realization methods 1. Flip Flop and gates 2. ROM, 3. PLA, 4. One-Hot, 5. DEC-DFF, 6. MUX-DFF,	 **PPT** **PPT** **PPT** **PPT** **PPT** **PPT**
14	• Asynchronous counter design	**PPT**
15	**Datapath Components** 1. serial adders and subtractors with accumulator 2. design of binary multipliers and dividers 3. *Review*: Number system 4. Signed number representation 5. Comparators 6. N-bit Multiplexer 7. Arithmetic-Logic Unit (ALU) 8. Combinational Shifter 9. Multipliers and Divider 10. Register File 11. Counters and Timers 12. Fixed-Point Representation & Arithmetic 13. Floating-Point Representation & Arithmetic 14. Carry Lookahead Adder 15. Parallelism: Pipelining and Concurrency	 629 633 1-8 16 **PPT** **PPT** **PPT** **PPT** **PPT** **PPT** **PPT** **PPT** **PPT** **PPT** **PPT**

Note 1: ***Some topics from the course syllabus are not fully covered in any text book.***

Note 2: ***The descriptions and timelines contained in this syllabus are subject to change at the discretion of the Professor.***

• Safety Guidelines and Resources

The information contained in the following link lists the University's Policies and Procedures. We strictly adhere to these policies in this course.
UT Dallas Syllabus Policies and Procedures - The University of Texas at Dallas

Visit Comets United webpage to obtain the latest information on the University's guidance and resources for campus health and safety.

- **Class Participation**

Regular class participation is expected. Students who fail to participate in class regularly are inviting scholastic difficulty. Successful participation is defined as consistently adhering to university requirements, as presented in this syllabus. Failure to comply with these University requirements is a violation of the Student Code of Conduct.

- **Class Attendance**

Regular and punctual class attendance is expected. Students who fail to attend class regularly are inviting scholastic difficulties. It is recommended that students attend the lectures. In-person participation records may be used to assist the University or local public health authorities in performing CV-19 occurrence monitoring. Please note that in-person attendance consistently adhering to university requirements, including public safety requirements, as presented in this syllabus. Failure to comply with these University requirements is a violation of the Student Code of Conduct.

- **Class Materials**

All documents for this class will be made available on eLearning.