EE/CE 3320 - 001 Course Syllabus –University of Texas at Dallas

Course: 3320 – Digital Circuits, Spring 2025

Class Schedule and Meeting Rooms: Monday and Wednesday, 8:30AM – 9:45AM, JSOM 1.110

Instructor: Hossein Pedram

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Office: ECSN 4.320

Office Hours: Monday, Wednesday 10:00AM – 11:00AM & Tuesday, Thursday 2:00PM – 3:00PM

Website: www.elearning.utdallas.edu

Teaching Assistants: TBD

TA Email: TBD

TA Office & Office hours: TBD

Course Pre-requisite/ Co- requisite: EE/CE 2310 / EE/CE 3120

Course Description:

Design and analysis of combinational logic circuits using basic logic gates and other building blocks like multiplexers and ROMs. Design and analysis of latches and flip-flops. Design and analysis of synchronous state machines. State minimization and introduction to state assignment. Design of datapath components: adders, multipliers, registers, shifters, and counters. Electrical properties of logic gates. Credit cannot be received for both courses, CS 4341 and CE 3320.

Student Learning Objectives/Outcomes:

- Ability to design, analyze, and optimize combinational logic circuits.
- Ability to design, analyze, and optimize synchronous sequential logic circuits.
- Ability to conduct timing analysis on combinational and sequential logic circuits.
- Ability to understand and apply practical aspects of digital design including datapath components.
- Ability to understand basic logic gate implementations and their electrical properties.

Required Textbook: Digital Design with RTL Design, VHDL, and Verilog, Frank Vahid, Second Edition, ISBN 978- 0-470-53108-2

Course & Instructor Policies:

- Besides office hours, the best and fastest way to reach me is via Emails. Please add EE/CE3320 in the subject of emails, so I can give priority to your emails.
- There will be a 5% penalty per day for late homework.

- The course is taught with the help of eLearning. The student should develop the habit of checking both eLearning and their UTD email often for assignments and announcements. Syllabus, lecture slides, homework, recordings, … will be posted on eLearning.
- Only emails sent from your official UTD email address or eLearning email will be considered and answered.
- EE/CE3320 Class Schedule, Sections 001, Spring 2025:

Week	Topic	Chapter
1	Review of Introduction to Digital Systems: Number systems, Gates, Gate implementation, Algebraic manipulations, Basic Boolean functions. Introduction to Verilog	1
2	Review of Introduction to Digital Systems: Minimization. Multiplexers, Decoders. Introduction to Verilog	2
3	Review of Introduction to Digital Systems: More on minimization. Adders. Verilog simulation	2
4	Adder/Subtractor Datapath. Comparator Datapath.	4
5	Introduction to Sequential Logic. Latches and Flip Flops.	3
6	Latches and Flip flops. Review of Exam 1 topics.	3
7	**Exam 1: Monday March 3, 2025 (in class)** Sequential logic	3
8	Finite State Machines (FSM) to describe sequential behavior	3
9	Controller design	3
10	Controller Design with Verilog. Basic registers	3
11	Datapaths: Registers, Counters, Timers	4
12	Datapaths: Registers, Counters, Timers	4
13	RTL Design	5
14	RTL Design	5
15	Review of Exam 2 topics **Exam 2: Wednesday May 7, 2025 (in class)**	

- NOTE: Some class lecture dates may be subject to change.

HW Sets:

HW 1	Introduction and Number Systems
HW 2	Combinational Circuits
HW 3	Combinational Circuits, Mux, Adders, Encoder/Decoder
HW 4	Adders, Comparators
HW 5	Latches and Flip Flops
HW 6	Registers and FSMs
HW 7	FSMs (Finite State Machines)
HW 8	More FSMs
HW 9	Registers
HW 10	Counters and Timers
HW 11	RTL Design

Grading Policy

Exam #1	30%
Exam #2	35%
Homework / Assignment	30%
Attendance	5%
In-class quizzes	5%

Grading Scale:

90 < A− < 93	93 < A < 97	97 < A+ < 100
80 < B− < 83	83 < B < 87	87 < B+ < 90
70 < C− < 73	73 < C < 77	77 < C+ < 80
60 < D− < 63	63 < D < 67	67 < D+ < 70
0 < F < 60		

UT Dallas Syllabus Policies and Procedures

The information below constitutes the University's policies and procedures segment of course syllabi, as described in http://go.utdallas.edu/syllabus-policies

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Technical Support:

If you experience any problems with your UT Dallas account, you may email assist@utdallas.edu or call the UT Dallas Computer Help Desk at 972-883-2911.

These descriptions and timelines are subject to change at the discretion of the instructor.