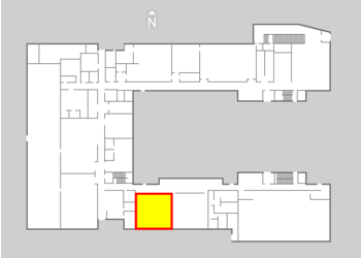
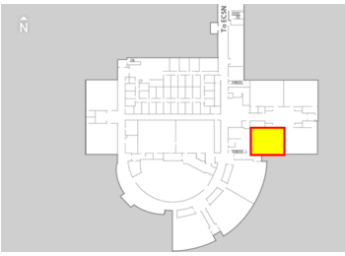
# COURSE SYLLABUS – CS/TE 4341 – FALL 2024

**Digital Logic and Computer Design**

**CS/TE 4341 – Section 001**
Monday & Wednesday
2:30 pm – 3:45 pm
Classroom: ECSW 1.365



**CS/TE 4341 – Section 502**
Monday & Wednesday
5:30 pm – 6:45 pm
Classroom: ECSS 2.312



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**Professor Contact Information**
Dr. Doug DeGroot
(972) 883-4200
doug.degroot@utdallas.edu
office: ECSS 4.409

**NOTE:** **Prof. DeGroot retains the right to modify this syllabus as the course progresses if he needs/desires to.**

**Office Info:**
Office Number: 4.409 in the ECSS building (the CS building).
Office hours: Monday/Wednesday from 1:00 – 2:00 P.M.

**Email:**
When/if you send me an email, please include a subject line like this:
**CS4341-<section>-<first name> <last name>-<anything else you want to include>**
Failing to do this may easily result in my failure to see your emails, as I rely on email filters to find all class emails. Please, please do this!

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**Course Prerequisites, Corequisites, and/or Other Restrictions**
**Prerequisites:**
CE 2310 or EE 2310 - Introduction to Digital Systems or
CS 3340 or SE 3340 or TE 3340 Computer Architecture
and PHYS 2326. Electromagnetism and Waves

**Corequisite:**
CS 4141 or TE 4141. (Same as TE 4341) Digital Systems Laboratory, to accompany CS 4341.

The purpose of the laboratory corequisite course is to give students an intuitive understanding of digital circuits and systems. Laboratory exercises include construction of simple digital logic circuits using prototyping kits and board-level assembly of a personal computer. Students that have credit for CS 2110 already have credit for this course and cannot get additional credit for this course.

**Restrictions:**
Credit cannot be received for both courses, (CS 4341 or TE 4341) and (CE 3320 or EE 3320).
Students that have completed CS 4340 cannot get credit for this course.

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**Course Description**

**CS 4341** - Digital Logic and Computer Design (3 semester credit hours) Boolean algebra and logic circuits; synchronous sequential circuits; gate level design of ALU, registers, and memory unit; register transfer operations; design of data path and control unit for a small computer; Input-Output interface.

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**Student Learning Objectives/Outcomes**

CLO 1: Ability to analyze, minimize and design gate-level combinational logic circuits using Boolean algebra and 3 and 4 variable Karnaugh Maps.

CLO 2: Ability to analyze and design simple synchronous sequential circuits

CLO 3: Ability to analyze, design and utilize digital logic components such as adders, multiplexers, decoders, registers, and counters.

CLO 4: Ability to understand RAM and ROM memory components, and utilize these in digital logic design

CLO 5: Ability to design computer components such as Arithmetic-Logic-Unit (ALU) and data path

CLO 6: Ability to understand the basics of hardware description languages such as Verilog or VHSIC Hardware Design Language (VHDL).

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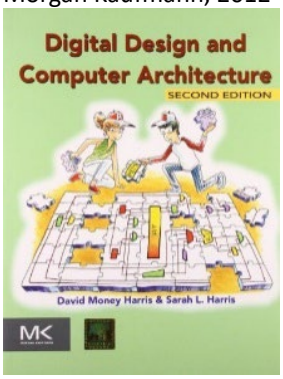
**Required Textbooks and Materials**

***Digital Design and Computer Architecture, 2nd Edition***
David M. Harris and Sarah L. Harris
Morgan Kaufmann, 2012




Some form of SystemVerilog:

I recommend using **EDAplayground**. You can find EDAplayground on the Web and use it for free, but you will need to sign up for a free account. **Please do that ASAP**. We will be using **Icarus Verilog 0.10**. I will upload a document to eLearning explaining how to get started with EDAplayground and Icarus Verilog

**Homework**
Homework will consist of problems that will need to be worked out **individually** by each student. Each student will solve their homework **on their own**. Collaboration is not allowed unless explicitly stated.

**Exams**
Exams will be a combination of simple problems, definitions, and diagram problems. Questions are allotted based on the nature of the material. Exams and home works will likely be comprehensive. I teach such that even all lectures are included in the exams. So be sure to attend and to take notes.

**Grading Scale** (the University's standard grading scale):

| 98-100 A+ | 88-89 B+ | 78-79 C+ | 68-69 D+ | Below 60 F |
|---|---|---|---|---|
| 92-97 A | 82-87 B | 72-77 C | 62-67 D | |
| 90-91 A- | 80-81 B- | 70-71 C- | 60-61 D | |

**Grading Policy (DeGroot retains the right to modify this weighting if he needs/desires to.)**

| Assignment | Weight |
|---|---|
| Homework 1 | 10 |
| Homework 2 | 10 |
| Homework 3 | 10 |
| Homework 4 | 10 |
| Exam 1 | 20 |
| Exam 2 | 20 |
| Exam 3 | 20 |

Classroom participation is also required. Failure to attend may result in loss of up to 5 grade points.

**Note:** CS 4141 (your lab class) is a separate class with a separate semester grade. I have nothing to do with that course.

**Homework Information:**

**Submitted homework files must be named as follows:**

HW<n>-CS4341-<your first and last names>.<ext>, where your file extension will be pdf, pdfx, doc, docx, etc.

Specific details of deliverables will be provided in each assignment write-up.

All homework assignments will be graded by the TA/Graders. **Therefore, if you have any questions at all concerning the homework assignments, please speak with the TA about it first.** Even if you were to approach Prof. DeGroot first, you would still have to go back to the TA. It will save us all time to start with the TA.

If you send email to your TA, please be sure to also cc: Prof. DeGroot on that email. And please adhere to the prescribed subject line contents as mentioned above.

If you are dissatisfied with the result of your meetings with a TA, then please send a new email to both your TA/grader and to Prof. DeGroot about that issue. Together, we can work to get it straightened out. You have every right to pursue any issue that concerns your grade in the course.

***Course & Instructor Policies***

**Late Work**

**Late assignments are not accepted without penalty - period**. Don't even ask! Assignments are due by the time stated at the top of the assignment write-up. When the submission instructions say "by midnight," don't worry if you are just a little late, like up to 15 minutes late. We will still accept it as being on time. But

please, no more than an that. This extra time is just to allow for possible submission problems such as Internet connection problems. It is NOT to allow for your being late in completing the homework.

**Suggestion**: Shoot to be done by Sunday 6:00 pm, not midnight, of the due date.

**Grade Disputes**

All grade disputes must be discussed & resolved by the student with the instructor within two weeks of posting any grade. But start with the TA (class grader) first!

**Classroom Citizenship**

Students are expected to be respectful to each other and to the course instructor. Disruptive behavior during lectures and talking among classmates is not tolerated.

## *ETHICAL BEHAVIOR*

Plagiarism is the unacknowledged incorporation of another's work into work which a student offers for credit. Using source code of another person's program, even temporarily or from the web, is considered plagiarism. Example: Someone putting their name on someone else's homework assignment and turning it in is cheating.

Collusion is the unauthorized collaboration of another person in preparing work that a student offers for credit. Allowing another person to use your source code, even temporarily, is considered collusion.

Example: Giving someone your homework, and then that person turns it in as their own work, then the giver is also guilty of cheating.

Dr. DeGroot's penalty for any form of dishonesty is a score of 0 on the entire assignment and a report to the Student Ethics Office.

**Comet Creed**

*This creed was voted on by the UT Dallas student body in 2014. It is a standard that Comets choose to live by and encourage others to do the same:*

*"AS A COMET, I PLEDGE HONESTY, INTEGRITY, AND SERVICE IN ALL THAT I DO."*

**UT Dallas Syllabus Policies and Procedures**

The information contained in the following link constitutes the University's policies and procedures segment of the course syllabus. It is included here by reference.

Please go to http://go.utdallas.edu/syllabus-policies for these policies.

**Students with Disabilities**

It is the policy and practice of The University of Texas at Dallas to make reasonable accommodations for students with properly documented disabilities. However, written notification from the Office of Student AccessAbility (OSA) is required. If you are eligible to receive an accommodation and would like to request it for this course, please discuss it with me via email and allow one week advance notice. Students who have questions about receiving accommodations, or those who have, or think they may have, a disability (mobility, sensory, health, psychological, learning, etc.) are invited to contact the Office of Student AccessAbility for a confidential discussion. OSA is located in the Student Services Building, suite 3.200. They can be reached by phone at (972) 883-2098, or by email at *studentaccess@utdallas.edu*.

**Course & Instructor Policies**

**Late Work**
No late homework submissions will be accepted. Don't even ask. (But see above.)

**Make Up Exams**

- If a student sits any exam, this means the student accepts the responsibility for that exam. Once taken, the exam will not be given again, and no make-up will be scheduled.
- If a student cannot make any interim exam, and the student brings adequate documentation of why they did not attend, (such as a doctor's note), then the Final Exam score will be substituted for the midterm.
- End of semester travel arrangements are not an acceptable reason for missing the Final Exam.
- If the student does miss the Final Exam, and the student brings adequate documentation of why they did not attend, (such as a signed doctor's note), a grade of Incomplete will be given and a make-up exam will be scheduled. If this action is not taken, the Final Exam will be a zero.

*A dental appointment or other non-emergency health situation is not an acceptable excuse for missing an examination you know about months in advance.*

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**Attendance Policy**
We will resume the standard UTD attendance policy and requirements this semester. Attendance will likely be taken each class. The following rules apply to total semester attendance.

Any student missing 3 *consecutive* class meetings will automatically lose one full letter grade.
Any student missing 4 *consecutive* class meetings will automatically fail the class.
Any student missing 4 or more classes, *whether consecutive or not,* will automatically lose one full letter grade (10 points).

**Additional Attendance Policies:**
Students who miss class must have a valid reason for not attending class. The situation should be clearly described in an e-mail sent directly to Dr. DeGroot. For medical issues, a doctor's note is the ***required*** form of proof. If you are sick, go to the doctor and get a note.

*Being late for class because of parking is not a valid excuse.*

If a student must travel to attend conferences, present papers, contests, or defend their work and the instructor is informed in advance, then the attendance will be forgiven for those dates. Traveling without an acceptable academic justification will not be accepted.

**DO NOT ASK TO BE PUT ON THE ROLL/ATTENDANCE SHEET AFTER THE ROLL CALL HAS BEEN CLOSED.**
**YOU WILL NOT BE PUT ON THE ROLL. ROLL CALL WILL GENERALLY BE OPEN THE FIRST 10 MINUTES OF A CLASS PERIOD.**
**Please be on time, always!**

# Schedule

The following dates and topics constitute your **READING, HW, and Exam** schedule. They aren't necessarily the same as the in-class topic discussions/lectures. **I retain the rights to modify the order, content, and schedule of lectures, exams, and homeworks as the semester progresses.**

| Date | Chapter | Topic, Assignment, Due Date(s), Exam Date(s) | HW / Projs | Class # |
|---|---|---|---|---|
| 19-Aug | 1 | Ch.1 - Digital Abstraction, numbers, gates | | 1 |
| 21-Aug | 1 | | | 2 |
| 26-Aug | 2 | Ch.1&2 - Combinational Circuits, Boolean Algebra | | 3 |
| 28-Aug | 2 | | | 4 |
| **2-Sep** | **3** | **LABOR DAY** | | |
| 4-Sep | 3 | Ch.2 - Circuit Optimization | HW1 out | 5 |
| 9-Sep | 4 | Ch.2 - Karnaugh Maps | | 6 |
| 11-Sep | 4 | Ch.2 - Muxes, Decoders, et al | | 7 |
| 16-Sep | 5 | Ch.2 - Muxes, Decoders, et al | | 8 |
| 18-Sep | 5 | | | 9 |
| 23-Sep | 6 | Ch.3 - Sequential Logic | | 10 |
| 25-Sep | 6 | | HW 2out | 11 |
| 30-Sep | 7 | **EXAM 1 (In Class)** | Exam 1 | 12 |
| 2-Oct | 7 | Ch.3 - Sequential Logic & FSMs | | 13 |
| 7-Oct | 8 | Ch.3 - Sequential Logic & FSMs | | 14 |
| 9-Oct | 8 | Ch.3 - Sequential Logic Building Blocks | | 15 |
| 14-Oct | 9 | Ch.4 - Hardware Description Languages | | 16 |
| 16-Oct | 9 | | HW 3 out | 17 |
| 21-Oct | 10 | Ch.5 Digital Building Blocks | | 18 |
| 23-Oct | 10 | | | 19 |
| 28-Oct | 11 | Ch.5 Digital Building Blocks | | 20 |
| 30-Oct | 11 | Ch.4&5 - Digital Building Blocks, Verilog | | 21 |
| 4-Nov | 12 | Ch.4&5 - Digital Building Blocks, Verilog | | 22 |
| 6-Nov | 12 | **EXAM 2 (In Class)** | Exam 2 | 23 |
| 11-Nov | 13 | ALUs in total, More Parallelism | HW4 out | 24 |
| 13-Nov | 13 | Floating-Point Math (bleh!) | | 25 |
| 18-Nov | 14 | Memories, PLA, and FPGAs | | 26 |
| 20-Nov | 14 | More Memories & FSMs | | 27 |
| 25-Nov | 15 | Misc Topics / Student Presentations | | 28 |
| **Nov 25-29** | **15** | **FALL BREAK** | | |
| 2-Dec | 16 | Misc Topics / Student Presentations | | 29 |
| 4-Dec | 16 | **EXAM 3 (in Class) (free Kleenex)** | Exam 3 | 30 |