Course Syllabus

CS/SE 2340 Computer Architecture, section 8, Spring 2024
Electrical and Computer Engineering
Erik Jonsson School of Engineering & Computer Science at UTD

Professor: Tooraj Nikoubin
Tooraj.Nikoubin@utdallas.edu
Office Hours: W 12noon-1pm by appointment
Room: ECSN 3.904, Teams
Phone: (972) UTD-4759

Location: FN 2.102
Time: TTh 08:30am – 09:45am

Course Description

CS/SE 2340 is an introductory course in computer organization and architecture, including system numbers, instruction set design, Datapath and control, pipelining, memory hierarchy, input/output, and parallelism. The trade-offs between hardware and software and performance evaluation and optimization of computer systems are included in this course. MIPS as an example of a RISC architecture will be used for understanding the architecture and processing data, along with programing in assembly language.

Course Pre-requisites

Prerequisites: CE/CS/TE 1337 or equivalent, and CE/CS/TE 2305 or equivalent

Course Learning Objectives

By the end of this course, you will be able to:

- Be able to write a fully functional, stand-alone medium size assembly language program (e.g. a basic Telnet client)
- Have an ability to represent numbers in and convert between decimal, binary, and hexadecimal and perform calculations using 2's complement arithmetic.
- Understand the basic model of a computer including the datapath, control, memory, and I/O components.
- Be able to program efficiently in an assembly level instruction set, including the use of addressing modes and data types.
- Understand the role of compilers, assemblers, and linkers and how programs are translated into machine language and executed.
- Be able to demonstrate comprehension of a pipelined architectures including datapaths and hazards.
- Be able to demonstrate comprehension of computer performance measures and their estimation.
- Understand the memory hierarchy including caches and virtual memory.

Course Material

- Required Textbook: David A. Patterson and John L. Hennessy, Computer Organization and Design: The Hardware/Software Interface, 5th Edition, Patterson and Hennessey, Morgan Kaufmann.
- RISC ASSEMBLER/SIMULATOR: This course uses the MARS MIPS assembler and simulator. MARS is available, free, for download from the following link: http://courses.missouristate.edu/kenvollmar/mars/
- Some of course materials are not available on Textbook, students should study them from PDF class lectures and note taking can help to complete the references.
- All announcements and homework assignments will be posted online for this course. It is the responsibility of each student to check this web page for new announcements and homework.
- You are expected to read the assigned chapters before each class, and to have the textbook to use as reference. The textbook also contains exercises and problems that you can use for self-study and practice.

● Academic Calendar

- First Class Day: Tuesday, Jan 16th, 2024
- Last Class Day: Friday, May 3rd, 2024
- Spring Break: March 11th to 17th
- 1st Exam: will be announced one week before exam,
- 2nd Exam: will be announced one week before exam,
- 3rd Exam: University Final Exam schedule (TBA)

● Course Announcements and Homework Assignments

Course announcements and homework assignments will be posted on eLearning for this course. Sometimes homework provides practice to solve difficult problems. Students are welcome to discuss homework with the instructor and teaching assistants.

● Grading Policy

Final grades in this course will be based on several homework assignments, projects, and two examinations given throughout the semester and a final examination. No makeup examinations will be offered in this course. Any graded work can be disputed in writing *within one week* of the return of that work. Complete work will be re-graded.
The grading policy is:

#	Items	Grade %
1	Test # 1	10%
2	Test # 2	15%
3	Final exam	30%
4	Project	15%
5	Homework	20%
6	Participations and Quiz	10%

● UT Dallas Policies and Procedures

For all issues related to sharing confidential information, student conduct and discipline, academic integrity, student grievance, incomplete grade, and other student related university policies please refer to this page: http://go.utdallas.edu/syllabus-policies

● Course Modality and Expectations

a. Instructional Mode

The mode of instruction will be Traditional Classroom (in-person) in this semester for this class.

b. Course Platform

Please use eLearning for access to the notes, submission of assignments (including HWs, Project report and quizzes), grading, etc. in this course.

c. Expectations

Students are expected to attend all lectures in-person at UTD, to submit all assignments, projects and other course requirements shown in this course on time. Students are expected to conduct professionally in all interactions with the TA and the instructor for the course material and projects. Any violations of the university rules and regulations will be referred to the university committee on student conduct. Please see Student Code of Conduct for more information.

● Class Participation

Regular class participation is expected. Students who fail to participate in class regularly are inviting scholastic difficulty. Successful participation is defined as consistently adhering to university requirements, as presented in this syllabus. Failure to comply with these University requirements is a violation of the Student Code of Conduct.

- **Class Materials**

- **List of Topics (subject to base on the progress of the class)**

#	Topic	References
1	Introduction	Hennessey/Patterson: Appendix B Hennessey/Patterson: 1.1 – 1.5, 1.12, Additional material on eLearning
2	Systems numbers, Fixed point and Floating- point numbers	Hennessey/Patterson: 3.1, 3.2, 3.5 Additional material on eLearning
3	Data path components, Computer Architecture and Organization	Hennessey/Patterson: A.1 – A.5 Hennessey/Patterson: 2.1 – 2.5, 2.12 Additional material on eLearning
4	MIPS Assembly Language Instructions	Hennessey/Patterson: A.10 Hennessey/Patterson: 2.1 – 2.7 Additional material on eLearning
5	MIPS Assembly Language Programing	Hennessey and Patterson: A.9 Hennessey and Patterson: 2.1 – 2.7, 2.10 Additional material on eLearning MARS Tutorial
6	Register Transfer Language (RTL)	Hennessey and Patterson: 4.1 – 4.4 Additional material on eLearning
7	Control unit and control signals	Hennessey and Patterson: 4.1 – 4.4 Additional material on eLearning
8	RISC vs SISC Processors	Hennessey and Patterson: 4.1 – 4.4 Additional material on eLearning
9	Subroutines, Procedures and Stack	Hennessey and Patterson: 2.8 Additional material on eLearning
10	Performance Basics, CPI, Amdahl's Law	Hennessey/Patterson: 1.6 – 1.10 Additional material on eLearning
11	Introduction to pipelined operation and architecture	Hennessey/Patterson: 4.5 – 4.6 Additional material on eLearning
12	RISC Systems and Hazards in pipeline operations and Branch Prediction	Hennessey/Patterson 4.7 – 4.8 Additional material on eLearning
13	Memory Hierarchy and Cache memory	Hennessey/Patterson: 5.1 – 5.2 Additional material on eLearning
14	IO and Interrupts and DMA	Hennessey/Patterson: 4.9 Additional material on eLearning
15	Cache memory access techniques	Hennessey/Patterson: 5.1 – 5.4, 5.8 Additional material on eLearning
16	Virtual Memory	Lecture slides on eLearning

***Note 1:** Some topics from the course syllabus are not fully covered in any textbook.*

***Note 2:** The descriptions and timelines contained in this syllabus are subject to change at the discretion of the Professor.*

- **CSMC**

The Computer Science Mentoring Center (CSMC) is a free resource available to all students taking this class. The CSMC provides assistance in many areas including:

- Understanding core concepts related to this class
- Developing a logical framework for a program
- Connecting programming constructs to the logic of the program
- Assisting in solving syntax and logical errors in your code
- Exam reviews and reworks (by faculty request)

The mentors will meet with you 1-on-1 to address your specific problem areas. Their goal is to help you understand what is wrong and how to fix it, but they will not do the work for you. For more information about the CSMC, including location and hours of operation, please visit http://csmc.utdallas.edu