Course syllabus

EE/CE 2310 Introduction to DIGITAL SYSTEMS, Summer 2022

Electrical and Computer Engineering

Erik Jonsson School of Engineering & Computer Science at UTD

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Office Hours: 2pm-3pm Th
by appointment on Teams/Webex
Office/Phone: ECSN 3.904, (972) UTD-4759

Location: JSOM 2.102
Lecture Time: TuTh 03:00pm – 05:15pm
Lab Time: Tu 10:00am – 02:15am

TA: TBA

Course Description

The importance of digital circuits and systems cannot be overestimated in present day and age. Digital circuits and systems form the basis for most of the electronic devices ranging from small electronic toys to large scale computers. Hence it is useful to understand how these circuits are designed and operate. All digital circuits and systems operate using the same concepts that will be presented in this class. The only difference is in the complexity of the circuits.

Course Pre-requisites

A working knowledge of basic algebra and knowledge of programming fundamentals.

Course Learning Objectives

- Be fluent in system numbers contains Binary numbers, Octal numbers, Hexadecimal numbers and base conversion,
- Boolean algebra and ability to apply Boolean algebra for function simplification
- Ability to design, analyze, and optimize of combinational logic circuits
- Ability to conduct timing analysis on combinational logic circuits
- Ability to Read and write assembly language codes and programing
- Have a basic knowledge of computer organization and design

Course Material

- **Required Text Book:**

- Charles H.Roth, Jr. and Larry L. Kinney, "Fundamentals of Logic Design"

- **References:**

- Frank Vahid: *Digital Design –with RTL Design, VHDL, and Verilog,* John Wiley Publishers. Second Edition, ISBN: 978-0-470-53108-2.
- S. Brown and Z. Vranesic, *Fundamentals of Digital Logic With Verilog Design*, McGraw-Hill Publishing. Second Edition, 2008

- All announcements and homework assignments will be posted online for this course. It is the responsibility of each student to check this web page at least once a week for new announcements and homework.

Academic Calendar

- First Class Day: Monday, May 23, 2022
- Last Class Day: Monday, Aug 8, 2022
- 1st Exam: will be announced one week before exam,
- 2nd Exam: will be announced one week before exam,
- 3rd Exam: Final Exam schedule TBA

- **Course Announcements and Homework Assignments**

Course announcements and homework assignments will be posted on the web page for this course. Sometimes homework provides practice to solve difficult problems. Students are welcome to discuss homework with the instructor and teaching assistants.

- **Grading Policy**

Final grades in this course will be based on several homework assignments and two examinations given throughout the semester and a final examination. No makeup examinations will be offered in this course. Any graded work can be disputed in writing *within one week* of the return of that work. Complete work will be re-graded.
The grading policy is:

	Course Requirements and Corresponding Weight	
1	Test # 1	15%
2	Test # 2	15%
3	Final exam	25%
4	Lab Projects	20%
5	Homework and Quiz	25%

- **UT Dallas Policies and Procedures**

For all issues related to sharing confidential information, student conduct and discipline, academic integrity, student grievance, incomplete grade, and other student related university policies please refer to this page: http://go.utdallas.edu/syllabus-policies

- **Class Participation**

Regular class participation is expected regardless of course modality. Students who fail to participate in class regularly are inviting scholastic difficulty. A portion of the grade for this course is directly tied to your participation in this class.

- **Course Modality and Expectations**

a. Instructional Mode

The mode of instruction will be Traditional Classroom (in-person) in this semester for this class.

b. Course Platform

Please use eLearning for access to the notes, submission of assignments (including HWs, Project report and quizzes), grading, etc. in this course.

c. Expectations

Students are expected to attend all live lectures (or asynchronously), conducts experiments individually. TAs will be available in their office hours or by appointment for helping students. Collaboration with other students or any other individual is prohibited (when it is not approved by professor), demonstrate the ability to design, implement, and test circuits shown in this lab, and conduct professionally in all interactions with the TA and the instructor for the lab. Any violations of the university rules and regulations will be referred to the university committee on student conduct. Please see Student Code of Conduct for more information.

d. Asynchronous Learning Guidelines

There is no asynchronous mode of learning for this course (see COVID-19 Guidelines and Resources for exceptions due to COVID 19).

- **List of Topics (subject to base on the progress of the class)**

No.	Topic	Text Section # [Online Section #]
1	**Introduction**	PPT
2	**Digital Logic Design Fundamentals** a. Truth tables, b. Boolean algebra c. Algebraic manipulation d. Logic gates AND-OR, OR-AND, NAND, NOR, XOR, XNOR e. Logic minimization f. Expressing Functions with Minterms & Maxterms (SOP and POS forms) g. Karnaugh Map h. Karnaugh Map simplifications i. Transistor Level Realization of the logic gates j. Timing analysis of the circuits	 PP. 1-12, 36-52, pp. 94-104 pp. 134-153 PPT PPT PPT PPT PPT PPT
3	**Multi-level gate circuits** a. AND-OR, OR-AND (AOI & OAI) b. NAND-NAND & NOR-NOR configurations c. Other configurations	pp. 199-217 PPT 206 PPT
4	**Combinational circuit design and simulation** a. Design of the circuit with limited fan-in b. Gate delays and timing diagrams	pp. 229-242 229 232
5	**Multiplexers, Decoders, and Programable Logic Designs** a. Multiplexers b. Three-state buffers c. Decoders and Encoders d. Read-Only Memories e. Programable Logic devices f. Complex programable logic devices g. Field-Programable Gate Arrays c. Binary Adders and Subractors, d. Comparators	pp. 260-285 261 265 268 271 275 280 282 PPT PPT
6	**Combinational logic design using HDL (Verilog)** Design of Combinational blocks using Verilog	(Video Tutorials) PPT
7	**CPU, Memory, and I/O** **Processor Design** **Microcontrollers** **Microcontroller Communication**	PPT
8	**MIPS instruction codes** **Assembly Language Programming** **Stack**	PPT
9	**Introduction to Sequential circuits**	PPT

Note 1: ***Some topics from the course syllabus are not fully covered in any text book.***

Note 2: ***The descriptions and timelines contained in this syllabus are subject to change at the discretion of the Professor.***