Course Syllabus

Course Information

CS 4341.0U1 – Digital Logic and Computer Design

Term: Summer 2022
Days & Time and Location: TTh 3:00PM-5:15PM @ ECSS 2.203

Instructor Contact Information

Nhut Nguyen, Ph.D.
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Office hours: **by appointment via MS Teams**

Course Pre-requisites, Co-requisites, and/or Other Restrictions
EE 2310: Introduction to Digital Systems or CS 2340: Computer Architecture, and PHYS 2326: Electromagnetism and Waves. Students that have completed CS 4340 cannot get credit for this course.
Co requisite: CS 4141: Digital Systems Laboratory (1 semester hour) Laboratory to accompany CS 4341. The purpose of this laboratory is to give students an intuitive understanding of digital circuits and systems. Laboratory exercises include construction of simple digital logic circuits using prototyping kits and board-level assembly of a personal computer. Students that have credit for CS 2110 have credit for this course and cannot get additional credit for this course t.

Course Description

CS 4341: Digital Logic and Computer Design (3 semester hours)
This course focuses on topics required for hardware design of computer systems. Topics include Boolean algebra and logic circuits; combinational and synchronous sequential circuits; gate level design of digital building blocks, registers, and memory unit; register transfer operations; design of data path and control unit for a small computer; memory system, Input-Output (I/O) interfaces.

Students that have completed CS 4340 cannot get credit for this course.

Student Learning Objectives/Outcomes

The main objective of this course is to study topics leading to the understanding and ability to design a computer using digital logic circuits, starting from basic gates and elementary Boolean algebra.

After successful completion of this course, the student should have

- Ability to analyze, minimize and design gate-level combinational logic circuits using Boolean algebra and 3 and 4 variable Karnaugh Maps.
- Ability to analyze and design simple synchronous sequential circuits
- Ability to analyze, design and utilize digital logic components such as adders, multiplexers, decoders, registers, and counters.
- Ability to understand RAM and ROM memory components, and utilize these in digital logic design
- Ability to design computer components such as Arithmetic-Logic-Unit (ALU) and data path
- Ability to understand the basics of hardware description languages such as Verilog or VHDL.

Recommended Textbook:

"Digital Design and Computer Architecture" Second edition (2013), *Harris & Harris*, Morgan Kauffman, ISBN:978-0-12-394424-5.

Required Course Materials: To be discussed and provided in class.

Assignments & Academic Calendar

Exams: There will be two exams during the course, and the second exam is comprehensive. . ***All tests will be online test using eLearning at the Testing Center and registration is required.*** Test materials will be taken mainly from classroom lectures and require a clear understanding of topics discussed in class.

Assignments: There will be regularly assigned reading and homework. Reading assignments should be done before the class session.

Tentative Class Schedule

Session	*Date*	*Topic*	*Reading Assignment*	*Assignments*
1	May 24	Introduction Verilog – An introduction		
2	May 26	Chapter 1 Introduction; Logic Levels	Ch 1.1-8	HW #1
3	June 31	Chapter 2 Combinational Logic Design	Ch 2.1-4	
4	June 2	Chapter 2 Combinational Logic Design	Ch 2.5-9	
5	June 7	Chapter 3 Sequential Logic Design	Ch 3.1,2	HW#2
6	June 9	Chapter 3 Sequential Logic Design	Ch 3.3,4	
7	June 14	Chapter 3 Sequential Logic Design	Ch 3.5,6	HW #3
8	June 16	Chapter 4 Hardware Description Language	Ch 4.1-4	
9	June 21	Chapter 4 Hardware Description Language	Ch 4.5-9	HW #4
10	June 23	Chapter 5 Digital Building Blocks	Ch 5.1,2	
11	June 28	*Exam I review*		
12	June 30	**Exam I**		
13	July 5	Chapter 5 Digital Building Blocks	Ch 5.3-5	HW #5
14	July 7	Chapter 6 Architecture (Review of 3340 topics	Ch 6	
15	July 12	Chapter 7 Microarchitecture	Ch 7.1,2	HW #6
16	July 14	Chapter 7 Microarchitecture	Ch 7.3,4	
17	July 19	Chapter 7 Microarchitecture	Ch 7.5,7,8	
18	July 21	Chapter 8 Memory Systems	Ch 8.1,2	HW #7
19	July 26	Chapter 8 Memory Systems	Ch 8.3,4	
20	July 28	Chapter 8 Input and Output (I/O) Systems	Ch 8.5,7	
21	Aug 2	*Exam II review*		
22	Aug 4	**Exam II**		

Grading Policy

The grade each student earns from this class will be based on the following table:

Exam I	15%
Exam II	45%
Assignments	35%
Attendance	5%
Total	100%

Grades are assigned according to the scale on the right:

A	93.0 - 100
A-	90.0 - 92.9
B+	87.0 - 89.9
B	83.0 - 86.9
B-	80.0 - 82.9
C+	77.0 - 79.9
C	73.0 - 76.9
C-	70.0 - 72.9
D+	67.0 - 69.9
D	60.0 - 66.9
F	Below 60.0

Course & Instructor Policies

- **Attendance policy:** *missing **three or four** in-class exercises leads to **one letter grade drop**, missing **five** in-class exercises leads to **an F grade**.*
- *All exams will be at the Testing Center and **seat reservation is required**. Seat reservations must be made for each exam and should be done at the beginning of the semester. If you do not reserve your seat you will not be able to take the exam and I cannot do anything about it, so **do not email me if you cannot take an exam because you did not reserve your seat**.*
- *There will be no makeup exams under normal circumstances.*
- *No late homework or assignment will be accepted!*
- *I do not read e-Learning e-mails. Please use my UTD e-mail account above for any communications.*
- *Emails **must** include class/section numbers in the subject to help me locate you (I have multiple classes/sections in the semester.) **Emails without class/section information will be silently ignored.***

Class Materials

The instructor may provide class materials that will be made available to all students registered for this class as they are intended to supplement the classroom experience. These materials may be downloaded during the course, however, these materials are for registered students' use only. Classroom materials may not be reproduced or shared with those not in class, or uploaded to other online environments except to implement an approved Office of Student AccessAbility accommodation. Failure to comply with these University requirements is a violation of the Student Code of Conduct.

Classroom Conduct Requirements Related to Public Health Measures

UT Dallas will follow the public health and safety guidelines put forth by the Centers for Disease Control and Prevention (CDC), the Texas Department of State Health Services (DSHS), and local public health agencies that are in effect at that time during the Fall 2021 semester to the extent allowed by state governance. Texas Governor Greg Abbott's Executive Order GA-38 prohibits us from mandating vaccines and face coverings for UT Dallas employees, students, and members of the public on campus. However, we strongly encourage all Comets to get vaccinated and wear face coverings as recommended by the CDC. Check the Comets United: Latest Updates webpage for the latest guidance on the University's public health measures. Comets are expected to carry out Student Safety protocols in adherence to the Comet Commitment. Unvaccinated Comets will be expected to complete the Required Daily Health Screening. Those students who do not comply will be referred to the Office of Community Standards and Conduct for disciplinary action under the Student Code of Conduct – UTSP5003.

Class Attendance

The University's attendance policy requirement is that individual faculty set their course attendance requirements. Regular and punctual class attendance is expected. Students who fail to attend class regularly are inviting scholastic difficulty. In some courses, instructors may have special attendance requirements; these should be made known to students during the first week of classes.

Class Participation

Regular class participation is expected. Students who fail to participate in class regularly are inviting scholastic difficulty. A portion of the grade for this course is directly tied to your participation in this class. It also includes engaging in group or other activities during class that solicit your feedback on homework assignments, readings, or materials covered in the lectures (and/or labs). Class participation is documented by faculty. Successful participation is defined as consistently adhering to University requirements, as presented in this syllabus. Failure to comply with these University requirements is a violation of the Student Code of Conduct.

Class Recordings

Students are expected to follow appropriate University policies and maintain the security of passwords used to access recorded lectures. Unless the Office of Student AccessAbility has approved the student to record the instruction, students are expressly prohibited from recording any part of this course. Recordings may not be published, reproduced, or shared with those not in the class, or uploaded to other online environments except to implement an approved Office of Student AccessAbility accommodation. Failure to comply with these University requirements is a violation of the Student Code of Conduct.

Comet Creed

This creed was voted on by the UT Dallas student body in 2014. It is a standard that Comets choose to live by and encourage others to do the same:

"As a Comet, I pledge honesty, integrity, and service in all that I do."

Academic Support Resources

The information contained in the following link lists the University's academic support resources for all students.

Please see http://go.utdallas.edu/academic-support-resources.

UT Dallas Syllabus Policies and Procedures

The information contained in the following link constitutes the University's policies and procedures segment of the course syllabus.

Please go to http://go.utdallas.edu/syllabus-policies for these policies.

These descriptions and timelines are subject to change at the discretion of the Instructor.