THE UNIVERSITY OF TEXAS AT DALLAS
Erik Jonsson School of Engineering and Computer Science
Department of Electrical and Computer Engineering

EE/CE 3320: Digital Circuits

(Spring 2021, Tuesday and Thursday: 1:00–2:15 p.m. (North America, Central Standard Time (CST)), VIRTUAL Sessions Using **Microsoft Teams**)

1 General Information

- *Instructor:* Mehrdad Nourani
- *Office & Phone:* ECSN 4.924, 972-883-4391
- *E-mail (Webpage):* nourani@utdallas.edu (http://www.utdallas.edu/~nourani)
- *Online Office Hours:* Tuesday and Thursday 11:00 am–12:00 pm (North America, Central Standard Time (CST)), or by appointment; VIRTUAL Using **Microsoft Teams**.
- *Required Text: Digital Design with RTL Design, VHDL and Verilog*, Frank Vahid, John Wiley Publishers, 2nd Edition, 2011, ISBN: 978-0-470-53108-2; OR
  Digital Design, Roman Lysecky and Frank Vahid, zyBooks Online 978-1-394-08971-0; To access: (i) Sign in or create an account at learn.zybooks.com, (ii) Enter zyBooks code: UTDALLASEE3320NouraniSpring2021, and (iii) Subscribe.
- *Other References: Fundamentals of Digital Logic With Verilog Design*, Stephen Brown and Zvonko Vranesic, McGraw-Hill Publishing, Second Edition, 2008. *Digital Design Principles and Practices*, John F. Wakerly, Prentice Hall, Fourth Edition, 2006.
- *Course Web Page:* http://elearning.utdallas.edu/
- *Teaching Assistant:* To be announced.

2 Course Modality and Expectations

- **Instructional Mode:** Remote/Virtual according to the following description: **https://covid.utdallas.edu/students-families-info/spring-2021-registration/**.
- **Course Platform:**
  - Microsoft Teams (**https://www.microsoft.com/**) for synchronous sessions (real-time lectures at the scheduled class time).
  - Microsoft Stream (**https://www.microsoftstream.com/**) for asynchronous learning (any-time access to video recordings).
  - Elearning (**https://elearning.utdallas.edu/**) for course materials (slides, tutorials, homework, announcements, etc.).
- **Expectations:** Students will upload their project reports and assignments to Elearning. Exams will be administered through Elearning.
- **Asynchronous Learning Guidelines**: Asynchronous access will be provided to all through recorded lecture videos. General information (FAQ) regarding asynchronous mode can be seen at **https://covid.utdallas.edu/response/faq/#asynchronous**

COVID-19 Guidelines and Resources
The information contained in the following link lists the University's COVID-19 resources for students and instructors of record. Please see **http://go.utdallas.edu/syllabus-policies**.

3 Catalog Description

EE/CE 3320 Digital Circuits (3 semester hours).
Design and analysis of combinational logic circuits using basic logic gates and other building blocks like multiplexers and ROMs. Design and analysis of latches and flip-flops. Design and analysis of synchronous state machines. State minimization and introduction to state assignment. Design of datapath components: adders, multipliers, registers, shifters, and counters. Electrical properties of logic gates.
Credit cannot be received for both courses, CS 4341 and EE/CE 3320. Prerequisite: EE/CE 2310. (3-0) S.

4 Course Objective

The objective of this undergraduate level course is to introduce the design methodologies for digital circuits and systems. The importance of digital circuits and systems cannot be overestimated in present day and age. Digital circuits form the basis for most of the electronic devices ranging from small electronic toys to large scale computers. All digital circuits operate using the same concepts that will be presented in this class. The only difference is in the complexity of the circuits. It is expected that the students will acquire a clear understanding of the main techniques, design strategies and the optimizations that are involved. In particular, the following are the course learning objectives:

- **CLO1**: Ability to design, analyze, and optimize combinational logic circuits.
- **CLO2**: Ability to design, analyze, and optimize synchronous sequential logic circuits.
- **CLO3**: Ability to conduct timing analysis on combinational and sequential logic circuits.
- **CLO4**: Ability to understand and apply practical aspects of digital design including datapath components.
- **CLO5**: Ability to understand logic gate implementations and their electrical properties.

5 Grading

Grading will be based on three tests and homeworks as follows:

Homework/Projects	25%	(Likely due dates marked with *)
Test 1:	25%	(Thurs. 2/25/2021, 1:00 p.m.)
Test 2:	25%	(Thurs. 4/1/2021, 1:00 p.m.)
Test 3:	25%	(Thurs. 5/6/2021, 1:00 p.m.)

$90 \leq A- < 93$	$93 \leq A < 97$	$97 \leq A+ \leq 100$
$80 \leq B- < 83$	$83 \leq B < 87$	$87 \leq B+ < 90$
$70 \leq C- < 73$	$73 \leq C < 77$	$77 \leq C+ < 80$
$60 \leq D- < 63$	$63 \leq D < 67$	$67 \leq D+ < 70$
$0 \leq F < 60$		

Note: Per UTD requirements for B.S. degrees, a student must earn a grade of $C-$ or better in each of the "major requirements" courses.

6 Course Policies

- Homeworks/projects will be assigned throughout the semester, and will be due approximately once every 10 days. All reports should be submitted through elearning.
- A homework/project is considered **late** if it is turned in after the due date. There will be 20% per day penalty for late homeworks up to 3 days excluding weekends and holidays. Late homeworks and reports won't be accepted after 3 days.
- No makeup tests/homeworks/projects will be offered in this course. Any graded work can be disputed in writing within one week of the return of that work. In such cases, the entire work will be regraded.
- Some of the homeworks are mini-projects and require Verilog programming and using CAD tools (mainly Xilinx Vivado toolset) for synthesis, simulation and analysis. This toolset is currently available for free download and/or through remote login (e.g. using NX Client or Xmanager or NoMachine) to UTD servers. To have enough time start as early as possible.
- Copying on examinations, assignments and projects is cheating and is prohibited. Any instances of cheating or plagiarism is considered academic dishonesty and will be subject to disciplinary penalties according to the UT Dallas policy on scholastic dishonesty. The penalties include the possibility of failure in the course and/or dismissal from the University. Since such dishonesty harms the individual, all students and the integrity of the University, policies on scholastic dishonesty will be strictly enforced. Please read carefully this policy in **http://www.utdallas.edu/deanofstudents/dishonesty/**.
- There is no make-up test or homework in this course. Under exceptional circumstances (e.g. hospitalization), official documentation is required and the University policies and procedures will be followed.
- Announcements and complementary materials will be posted on the course web page. However, regular attendance and taking notes are highly recommended.

7 Syllabus & Tentative Lecture Plan

Weeks		*Readings from Text OR [zyBooks Online]*	*Topics Coverage*
Tue.	*Thur.*		
1/19	1/21	1.1-1.3 [1.2-8] 2.4-2.6	Introduction: course introduction; technologies and style; Logic Gates and Implementations: review of basic logic functions;
1/26	1/28*	2.1-2.3 [1.1-2] A.1-A.3	electrical properties of logic gates; CMOS implementation of logic gates; Digital Logic Design Fundamentals: review of truth tables,
2/2	2/4	2.6-2.8, pp. 419-422 [1.2,2.6-7]	boolean algebra and algebraic proofs; AND-OR, OR-AND, NAND, NOR circuits;
2/9*	2/11	9.1, 9.2 [7.1-4] 6.1, 6.2 [1.9-12, 2.1-5, 2.10-12]	combinational logic design using Verilog; logic minimization (SOP and POS forms);
2/16	2/18*	2.10 (pp. 91-92) [1.5] 2.9, 2.10 (pp. 93) [2.8-9]	Combinational Logic Analysis and Design: functional and timing analysis; decoders and encoders; multiplexers and demultiplexers;
2/23	2/25	5.7 (pp. 292, 308-309) [6.9]	programmable logic devices; **TEST 1** (Fundamentals & Combinational Logic)
3/2	3/4	pp. 424-431, pp. 227 [6.4] 3.2 [3.1-2]	ROM based logic design; Field Programmable Gate Arrays; tristate logic; Sequential Logic Elements: latches and flip-flops;
3/9*	3/11	3.5 (pp. 146-150), 4.2 [3.2,3.12,4.6] 3.4 (pp. 140), 6.3 (pp. 360) [3.3-6]	latch and flip-flop timings; registers Sequential Logic Analysis and Design: sequential logic analysis;
3/16	3/18		**Spring Break – University Holiday**
3/23	3/25*	3.3, 3.4 [3.7-11] 9.3 (pp. 502, 504, 506) [7.5-6]	sequential logic design; sequential logic design using Verilog;
3/30	4/1	5.5 [3.12]	sequential logic circuit timing; **TEST 2** (Sequential Logic)
4/6	4/8*	6.3 [3.8-9] 1.2 (pp. 11-21), B.2 [1.10,9.4-5]	state minimization and state encoding (assignment); Arithmetic Circuits: review of number system;
4/13	4/15	4.6 (pp. 200) [4.2,9.3] 4.3, 4.6, 9.4 (pp. 510, 512, 515) [4.1-3]	signed number representation; adders and subtracters;
4/20*	4/22	4.4, 4.5, 4.7, 4.8 [4.4-5,6.3,6.6] 4.9, 4.10 [4.6,6.4-5]	comparators; multipliers; Arithmetic Logic Units; combinational shifters; counters; timers; register files;
4/27	4/29*	B.3, B.4 [9.6-7] 9.5, pp. 234, C.1-C.3	fixed-point and floating-point representation and arithmetic; Digital Design Examples: combinational and sequential case studies;
5/4	5/6	6.4, 6.5 (pp. 377-380), Miscellaneous	Advanced Topics: carry lookahead adder, parallelism (pipelining, concurrency); digital circuit testing; **TEST 3** (Comprehensive)

Notes: Some topics in this course syllabus are not fully covered in any text book. Dates with "*" indicate likely due date of homework/projects.

8 Comet Creed

This creed was voted on by the UT Dallas student body in 2014. It is a standard that Comets choose to live by and encourage others to do the same: **"As a Comet, I pledge honesty, integrity, and service in all that I do."**

9 UT Dallas Syllabus Policies and Procedures

The information contained in the following link constitutes the University's policies and procedures segment of the course syllabus. Please go to **http://go.utdallas.edu/syllabus-policies** for these policies.

The descriptions and timelines contained in this syllabus are subject to change at the discretion of the Professor.