EE / CE 3320.003: DIGITAL CIRCUITS

Spring* 2021** | ***TR* 10:00am – 11:15am** | ***Remote / Virtual

Instructor: Poras T. Balsara
(972) 883-2557, poras@utdallas.edu
Office Hrs: TR 11:30am – 12:30pm or by appointment
(Use Join The Meeting link from eLearning)

TA: *to be announced*

Course Platform: Microsoft Teams (Use Join The Meeting link from eLearning)
Asynchronous Learning Guidelines: https://www.utdallas.edu/covid/response/faq/#asynchronous
Students opting for completely asynchronous option must declare and understand instructions.

- **Course Description**

The importance of digital circuits and systems cannot be overestimated in present day and age. Digital circuits form the basis for most of the electronic devices ranging from small electronic toys to large scale computers. Hence it is useful to understand how these circuits are designed and operate. All digital circuits operate using the same concepts that will be presented in this class. The only difference is in the complexity of the circuits.

- **Course Pre-requisites**

Prerequisites: EE 2310

- **Course Learning Objectives**
  - Ability to design, analyze, and optimize combinational logic circuits
  - Ability to design, analyze, and optimize synchronous sequential logic circuits
  - Ability to conduct timing analysis on combinational and sequential logic circuits
  - Ability to understand and apply practical aspects of digital design including datapath components
  - Ability to understand logic gate implementations and their electrical properties

- **Course Material**
  - **Required Text Book:**
    - Frank Vahid: *Digital Design –with RTL Design, VHDL, and Verilog,* John Wiley Publishers. Second Edition, ISBN: 978-0-470-53108-2.

      OR
    - Roman Lysecky and Frank Vahid: *Digital Design*. zyBooks Online (978-1-394-07174-6). In order to access this book please follow these instructions:
      1. Sign in or create an account on **learn.zybooks.com**
      2. Enter zyBook code: **UTDALLASEE3320BalsaraSpring2021**
      3. Subscribe
  - **Online Course Material: http://eLearning.utdallas.edu**
  - **References:**
    - S. Brown and Z. Vranesic, *Fundamentals of Digital Logic with Verilog Design*, McGraw-Hill Publishing. Second Edition, 2008

- **Academic Calendar**

First Class:	Tuesday, January 19, 2021
Last Class:	Thursday, May 6, 2021
Spring Break:	March 15 to March 21, 2021
1st Exam:	Thursday, February 18, 2021
2nd Exam:	Thursday, March 25, 2021
3rd Exam:	Thursday, May 6, 2021

- **Course Announcements and Homework Assignments**

Course announcements and homework assignments will be posted on the eLearning page for this course and will not be handed out in the class. It is student's responsibility to download and solve homework in time. Homework must be turned in on time. Homework provides practice to solve difficult problems. Students are welcome to discuss homework with the instructor and teaching assistants.

- **Grading Policy**

Final grades in this course will be based on several homework assignments and examinations given throughout the semester. No makeup examinations will be offered in this course. Any graded work can be disputed in writing *within one week* of the return of that work. Complete work will be re-graded. The grading policy is:

Homework:	20%
First Examination:	27%
Second Examination:	27%
Third Examination:	26%

- **Class Participation**

Regular class participation is expected. Students who fail to participate in class regularly are inviting scholastic difficulty. It also includes engaging in group or other activities during class that solicit your feedback on homework assignments, readings, or materials covered in the lectures (and/or labs).

- **Class Recordings**

Students are expected to follow appropriate University policies and maintain the security of passwords used to access recorded lectures. Unless the Office of Student AccessAbility has approved the student to record the instruction, students are expressly prohibited from recording any part of this course. Recordings may not be published, reproduced, or shared with those not in the class, or uploaded to other online environments except to implement an approved Office of Student AccessAbility accommodation. Failure to comply with these University requirements is a violation of the Student Code of Conduct.

- **Class Materials**

The Instructor may provide class materials that will be made available to all students registered for this class as they are intended to supplement the classroom experience. These materials may be downloaded during the course; however, these materials are for registered students' use only. Classroom materials may not be reproduced or shared with those not in class, or uploaded to other online environments except to implement an approved Office of Student AccessAbility accommodation. Failure to comply with these University requirements is a violation of the Student Code of Conduct.

- **Technical Requirements**

In addition to a confident level of computer and Internet literacy, certain minimum technical requirements must be met to enable a successful learning experience. Please review the important technical requirements on the Getting Started with eLearning webpage.

- **Distance Learning Student Resources**

This course can be accessed using your UT Dallas NetID account on the eLearning website. Please see the course access and navigation section of the Getting Started with eLearning webpage for more information. To become familiar with the eLearning tool, please see the Student eLearning Tutorials webpage.

UT Dallas provides eLearning technical support 24 hours a day, 7 days a week. The eLearning Support Center includes a toll-free telephone number for immediate assistance (1-866-588-3192), email request service, and an online chat service.

- **Distance Learning Student Resources**

Online students have access to resources including the McDermott Library, Academic Advising, The Office of Student AccessAbility, and many others. Please see the eLearning Current Students webpage for more information.

- **Server Unavailability or Other Technical Difficulties**

The University is committed to providing a reliable learning management system to all users. However, in the event of any unexpected server outage or any unusual technical difficulty which prevents students from completing a time sensitive assessment activity, the instructor will provide an appropriate accommodation based on the situation. Students should immediately report any problems to the instructor and also contact the online eLearning Help Desk. The instructor and the eLearning Help Desk will work with the student to resolve any issues at the earliest possible time.

- **Academic Support Resources**

The information contained in the following link lists the University's academic support resources for all students. Please go to Academic Support Resources webpage for these policies.

- **UT Dallas Comet Creed**

This creed was voted on by the UT Dallas student body in 2014. It is a standard that Comets choose to live by and encourage others to do the same:

"*As a Comet, I pledge honesty, integrity, and service in all that I do*."

- **UT Dallas Policies and Procedures**

The information contained in the following link constitutes the University's policies and procedures segment of the course syllabus. Please go to UT Dallas Syllabus Policies webpage for these policies.

NOTE: *The descriptions and timelines contained in this syllabus are subject to change at the discretion of the Professor.*

- **List of Topics** (with relevant section #s from the printed text book and the online book)

No.	Topic	Text Section # [Online Section #]
1	**Introduction**	1.1-1.3 [1.2-8]
2	**Digital Logic Design Fundamentals**	
	a. *Review*: Truth tables, Boolean algebra and algebraic proofs	2.4, 2.5, 2.6, A.1-A.3 (*self-study*)
	b. AND-OR, OR-AND, NAND, NOR, XOR, XNOR circuits	2.6-2.8, pp. 419-422 [1.2, 2.6-7]
	c. Combinational logic design using Verilog	9.1, 9.2 (*Verilog*) [7.1-4]
	d. Logic minimization (SOP and POS forms)	6.1, 6.2 [1.9-12, 2.1-5, 2.10-12]
3	**Combinational Logic Analysis and Design**	
	a. Functional and Timing analysis	2.10 (pp. 91,92) [1.5]
	b. Decoders and Encoders	2.9, 2.10 (pp. 93) [2.9]
	c. Multiplexers and Demultiplexers	2.9 [2.8]
	d. PLDs: ROM based logic design	5.7 (pp. 292,308), pp. 424-431 [6.9]
	e. Tristate Logic	pp. 227 [6.4]
4	**Sequential Logic Elements**	
	a. Latches and Flip-flops	3.2 [3.1-2]
	b. Latch and flip-flop timings	3.5 (pp. 146-150) [3.2, 3.12]
	c. Registers	4.2 [4.6]
5	**Sequential Logic Analysis and Design**	
	a. Sequential logic analysis	3.4 (pp. 140), 6.3 (pp. 360) [3.3-6]
	b. Sequential logic design	3.3, 3.4 [3.7-11]
	c. Sequential logic design using Verilog	9.3 (pp. 502, 504, 506) [7.5-6]
	d. Sequential logic circuit timing	5.5 [3.12]
	e. State minimization and State encoding (assignment)	6.3 [3.8-9]
6	**Datapath Components**	
	a. *Review*: Number system	1.2, B.2 (*self-study*) [1.10, 9.4-5]
	b. Signed number representation	4.6 (pp. 200) [4.2, 9.3]
	c. Adders and Subractors	4.3, 4.6, 9.4, [4.1-3]
	d. Comparators	4.4 [4.4]
	e. N-bit Multiplexer	?.? [4.5]
	f. Arithmetic-Logic Unit (ALU)	4.7 [6.6]
	g. Combinational Shifter	4.8 [?.?]
	h. Multipliers	4.5 [6.3]
	i. Register File	4.10 [4.6, 6.4-5]
	j. Counters and Timers	4.9 [?.?]
	k. Fixed-Point Representation & Arithmetic	B.3 [?.?]
	l. Floating-Point Representation & Arithmetic	B.4 [9.6-7]
	m. *Advanced Topics*	
	• Carry Lookahead Adder	6.4
	• Parallelism: Pipelining and Concurrency	6.5 (pp. 377-380)
7	**Logic Gates Implementation**	2.1-2.3 [1.1-2]
	a. CMOS implementation of basic logic gates	…
	b. Electrical properties of logic gates	…
8	**Digital Design Examples**	9.5, pp. 234, C.1-C.3

Note: *Some topics from the course syllabus are not fully covered in any text book.*