



Course syllabus
EE/CE 3320 DIGITAL CIRCUITS, Fall 2020
Electrical and Computer Engineering
Erik Jonsson School of Engineering & Computer Science at UTD

Professor: Tooraj Nikoubin
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Office Hours: only by appointment

Location: Remote/Virtual
Time: TTh 05:30pm – 06:45pm
TA: TBA
TA Email: TBA

Room: ECSN 3.904, (972) UTD-4759

● Course Description

The importance of digital circuits and systems cannot be overestimated in present day and age. Digital circuits form the basis for most of the electronic devices ranging from small electronic toys to large scale computers. Hence it is useful to understand how these circuits are designed and operate. All digital circuits operate using the same concepts that will be presented in this class. The only difference is in the complexity of the circuits.

● Course Pre-requisites

Prerequisites: EE 2310

● Course Learning Objectives

- Ability to design, analyze, and optimize combinational logic circuits
- Ability to design, analyze, and optimize synchronous sequential logic circuits
- Ability to conduct timing analysis on combinational and sequential logic circuits
- Ability to understand and apply practical aspects of digital design including datapath components
- Ability to understand logic gate implementations and their electrical properties

● Course Material

○ Required Text Book:

- Charles H. Roth, Jr. and Larry L. Kinney, "Fundamentals of Logic Design"

○ References:

- Frank Vahid: *Digital Design –with RTL Design, VHDL, and Verilog*, John Wiley Publishers. Second Edition, ISBN: 978-0-470-53108-2.
- S. Brown and Z. Vranesic, *Fundamentals of Digital Logic With Verilog Design*, McGraw-Hill Publishing. Second Edition, 2008
- All announcements and homework assignments will be posted online for this course. It is the responsibility of each student to check this web page at least once a week for new announcements and homework.

● Academic Calendar

- First Class Day: Monday, Aug. 17, 2020
- Last Class Day: Wednesday, Nov. 25, 2020
- Thanksgiving: Nov. 26 to 29, 2020
- 1st Exam: Tuesday Sep 22th 5:30pm – 6:45pm,
- 2nd Exam: Tuesday Oct 27th 5:30pm – 6:45pm,
- 3rd Exam: Final Exam schedule TBA (Dec 2 to Dec 8)

- **Course Announcements and Homework Assignments**

Course announcements and homework assignments will be posted on the web page for this course. Sometimes homework provides practice to solve difficult problems. Students are welcome to discuss homework with the instructor and teaching assistants.

- **Grading Policy**

Final grades in this course will be based on several homework assignments and two examinations given throughout the semester and a final examination. No makeup examinations will be offered in this course. Any graded work can be disputed in writing *within one week* of the return of that work. Complete work will be re-graded.

The grading policy is:

Course Requirements and Corresponding Weight		
1	Test # 1	15%
2	Test # 2	15%
3	Final exam	35%
4	Project	10%
5	Homework and Quiz	25%

- **Class Recordings**

Students are expected to follow appropriate University policies and maintain the security of passwords used to access recorded lectures. Unless the Office of Student AccessAbility has approved the student to record the instruction, students are expressly prohibited from recording any part of this course. Recordings may not be published, reproduced, or shared with those not in the class, or uploaded to other online environments except to implement an approved Office of Student AccessAbility accommodation. Failure to comply with these University requirements is a violation of the Student Code of Conduct.

- **Class Participation**

Regular class participation is expected regardless of course modality. Students who fail to participate in class regularly are inviting scholastic difficulty. A portion of the grade for this course is directly tied to your participation in this class.

- **Course Platform**

For access to notes, live and taped lectures, submission of assignments, grading, etc. please use eLearning for this course. WebEx is also used during the scheduled class periods and office hours.

- **Asynchronous Learning Guidelines**

The class lectures will be delivered on eLearning live during class time.

The pre-record of lecture will be available and students can view the lecture after the lecture has been given live. If students selected asynchronous manner, they can use recorded lectures.

The HWs & Projects are conducted at home in an asynchronous manner (a due date for each case will be enforced for all modalities).

See link below for details regarding asynchronous access.

<https://www.utdallas.edu/fall-2020/asynchronous-access-for-fall-2020/>

- **UT Dallas Policies and Procedures**

For all issues related to sharing confidential information, student conduct and discipline, academic integrity, student grievance, incomplete grade, and other student related university policies please refer to this page:

<http://go.utdallas.edu/syllabus-policies>

• **List of Topics** (subject to base on the progress of the class)

No.	Topic	Text Section # [Online Section #]
1	Introduction	PPT
2	Digital Logic Design Fundamentals (Review) a. Review: Truth tables, Boolean algebra and algebraic proofs, AND-OR, OR-AND, NAND, NOR, XOR, XNOR circuits d. Logic minimization (SOP and POS forms) e. Karnaugh Map f. Transistor Level Realization of the logic gates g. Timing analysis of the circuits	PP. 1-12, 36-52, pp. 94-104 pp. 134-153 PPT PPT
3	Quine-McClusky Method	pp. 173-184
4	Multi-level gate circuits a. AND-OR, OR-AND (AOI & OAI) b. NAND-NAND & NOR-NOR configurations c. Other configurations	pp. 199-217 PPT 206 PPT
5	Combinational circuit design and simulation a. Design of the circuit with limited fan-in b. Gate delays and timing diagrams c. Hazards in combinational logic	pp. 229-242 229 232 240
6	Multiplexers, Decoders, and Programable Logic Designs a. Multiplexers b. Three-state buffers c. Decoders and Encoders d. Read-Only Memories e. Programable Logic devices f. Complex programable logic devices g. Field-Programable Gate Arrays c. Binary Adders and Subtractors, d. Comparators	pp. 260-285 261 265 268 271 275 280 282 PPT PPT
7	Coding a. BCD, Aiken, Excess 3, Gray, and some other codes b. Code converters (like Decimal to BCD convertor) c. 7-segment display d. Even parity and error detection e. BCD Adder and subtractor	PPT
8	Combinational logic design using Verilog Hamming with even parity (First Project)	(Video Tutorials) PPT
9	Latches and Flip-Flops, Buffer, shift Register a. Set-Reset Latch b. Gate Latches c. Edge-Triggered D Flip-Flop d. S-R Flip-Flop e. J-K Flip-Flop f. T Flip-Flop g. Buffer, Shift Register	pp. 331-354 338 342 346 349 350 351 380
10	Counters and Counter design a. Design of BCD Counter b. Design of Binary Counter c. Count up and Count down counter d. Counter design with D, T, RS and JK Flip-Flops e. Counters for other sequences	PPT 384 PPT 395 389
11	Analysis of clocked sequential circuits a. Frequency dividers b. Timing analysis of counters c. Timing analysis of synchronous and asynchronous circuits g. Sequential logic design using Verilog Programable Timer (Second Project)	PPT PPT PPT PPT Video Tutorial PPT
12	Derivation of state Graphs and State Tables (State Machines) a. Design of Sequence Detector	453-497 457

	d. More complex Design Problems e. Guidelines for Construction of State Graph f. Elimination of Redundant States g. Equivalent states h. Determination of state equivalence using an implication table i. Timing analysis of state machines	463 467 505 507 509 PPT
13	Datapath Components a. serial adders and subtractors with accumulator b. design of binary multipliers and dividers c. <i>Review</i> : Number system b. Signed number representation d. Comparators e. N-bit Multiplexer f. Arithmetic-Logic Unit (ALU) g. Combinational Shifter h. Multipliers and Divider i. Register File j. Counters and Timers k. Fixed-Point Representation & Arithmetic l. Floating-Point Representation & Arithmetic	629 633 1-8 16 PPT PPT PPT PPT PPT PPT PPT PPT PPT PPT
14	Advanced Topics • Race, CLK-Skew • Carry Lookahead Adder • Parallelism: Pipelining and Concurrency	PPT PPT PPT

Note 1: *Some topics from the course syllabus are not fully covered in any text book.*

Note 2: *The descriptions and timelines contained in this syllabus are subject to change at the discretion of the Professor.*